

https:// github.com/ RedBalloonShena nigans/ MonitorDarkly

A Monitor Darkly

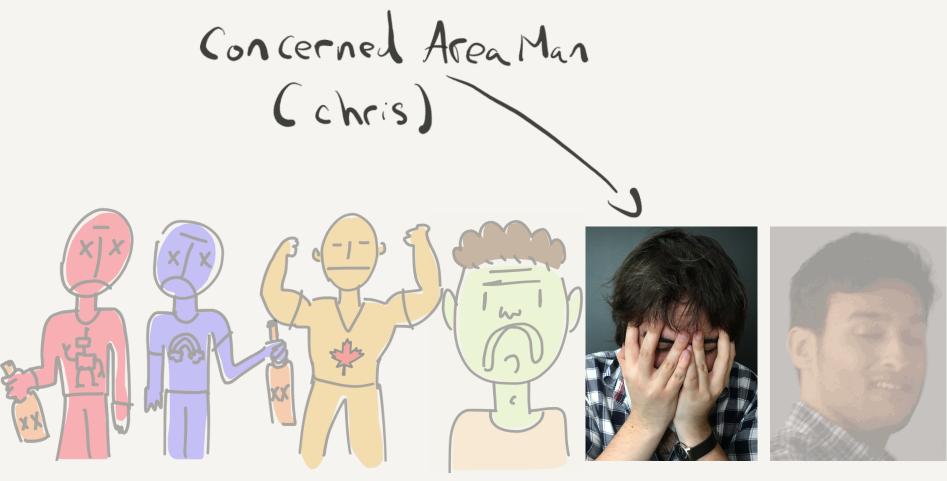
Ang Cui, PhD Jatin Kataria





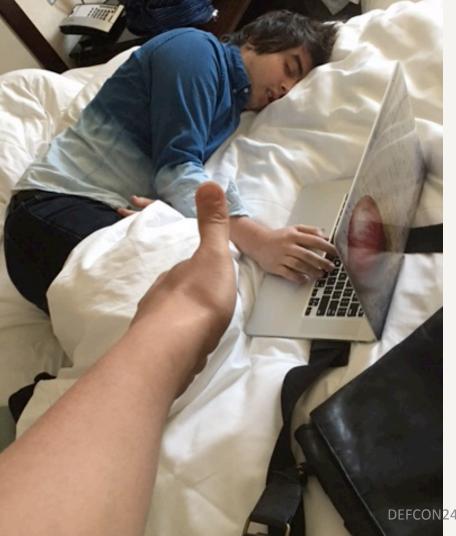






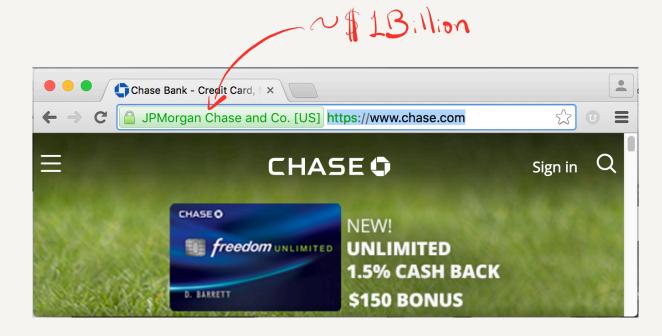




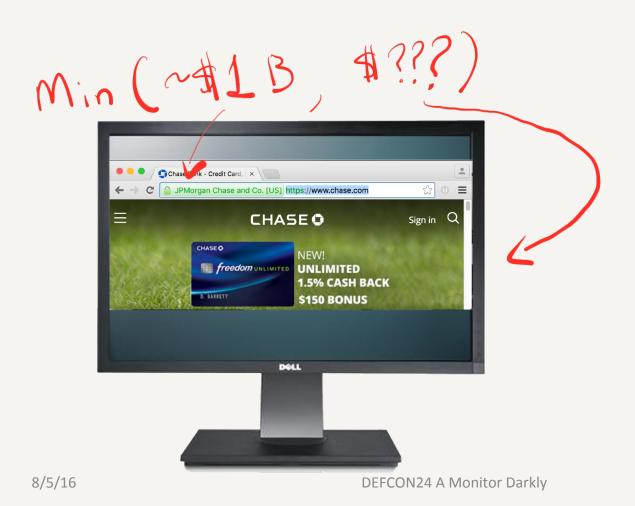


A Good Hacker ISA LAZY HACKER









Dell Whon, I can haz





like 1 minute of googling.... 9009 p



Verified Answer

Error = No TUSB3410 boot device

Discussion = This does not effect the monitor functionality. It only applies if we decide to do a firmware update

Solution =

* Go here



- * Download/save "TI WDF USBUART Single Driver (Rev. A)" zip file (sllc428a.zip) to your windows desktop
- * Unzip the file into its own folder
- * Open the folder and run "TI_WDF_USBUART_SINGLE_DRIVER_V6.7.2.0_WHQL.exe"
- * It should create the following folder:

C:\Program Files (x86)\Texas Instruments Inc\TI_WDF_USBUART_SINGLE_DRIVER_V6.7.2.0_WHQL

* Run Setup









We both already have Sweet monitors. No one will miss that 34 inch





These Monsters have no heart y

There will be no END to their senseless Savagery (and I have a million VIM plugins!)



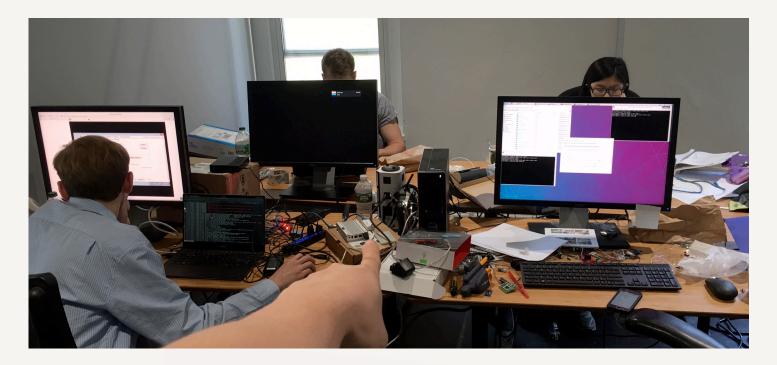


8/5/16

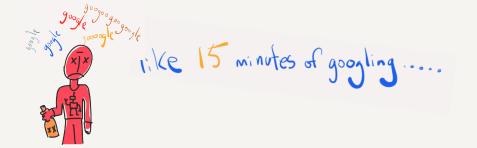


Interns





Interns get Dell U2410's so....



[PDF] DELL U2410 USB FW Upgrade Instruction

https://forum-en.msi.com/index.php?action=dlattach;topic=165660.0;attach... -

firmware upgrade.) Desktop & Notebook: 2. Connect the power cord and turn on the. U2410 monitor-tobe flashed. 3. Connect USB uplink cable from the. 3. Connect USB uplink cable from the computer USB port to U2410 USB upstream port.



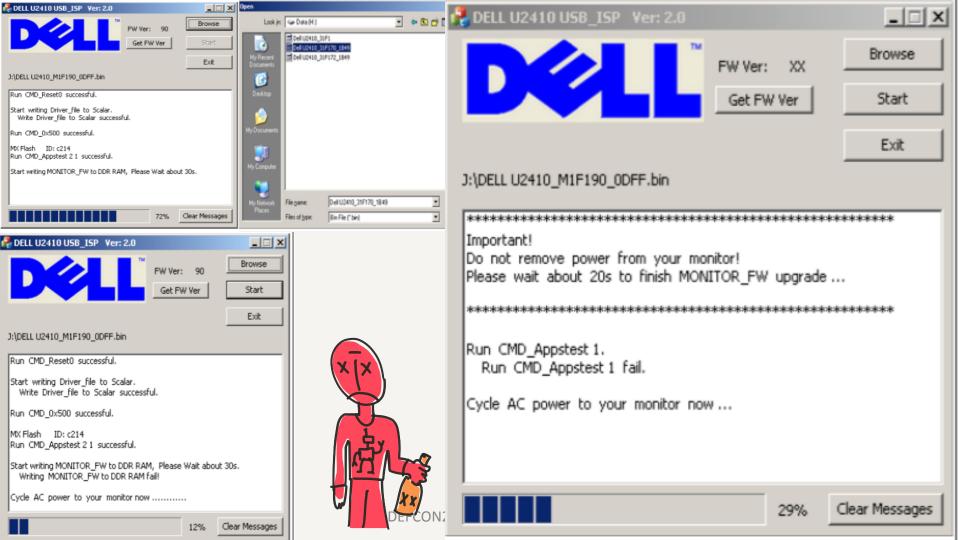
U2410 ISP Tool 2.0

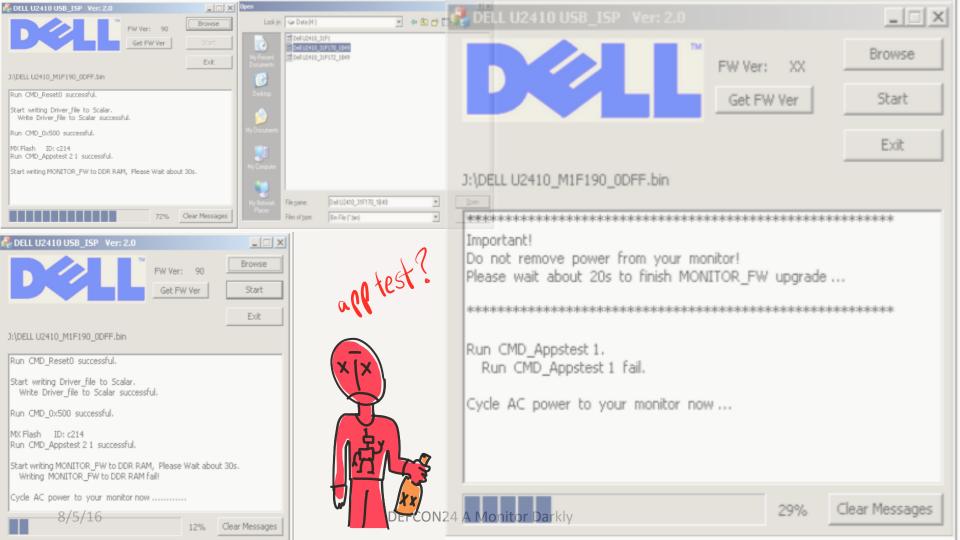


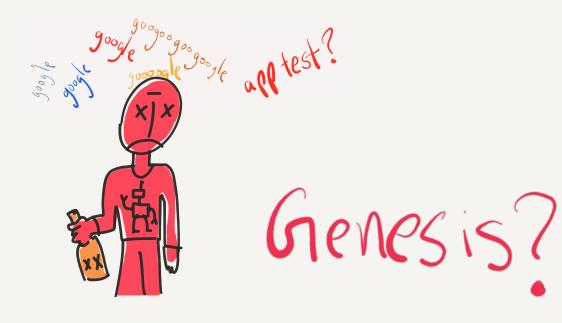
Double click
 " U2410 ISP TOOL
 2.0 " package to start

installation ..







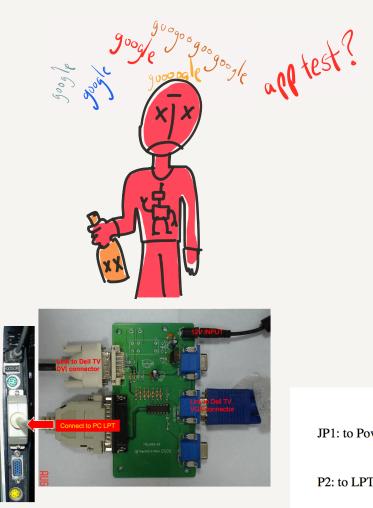


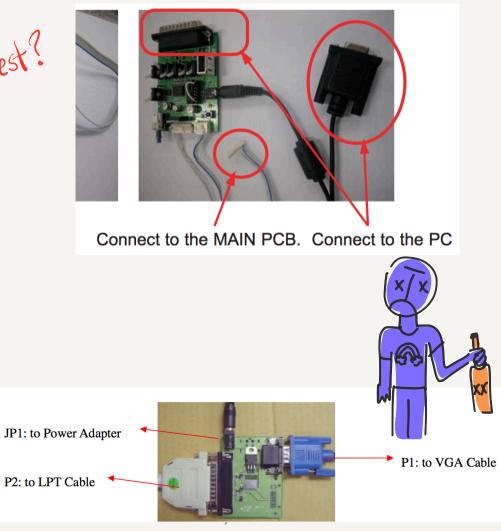




Grobe 3





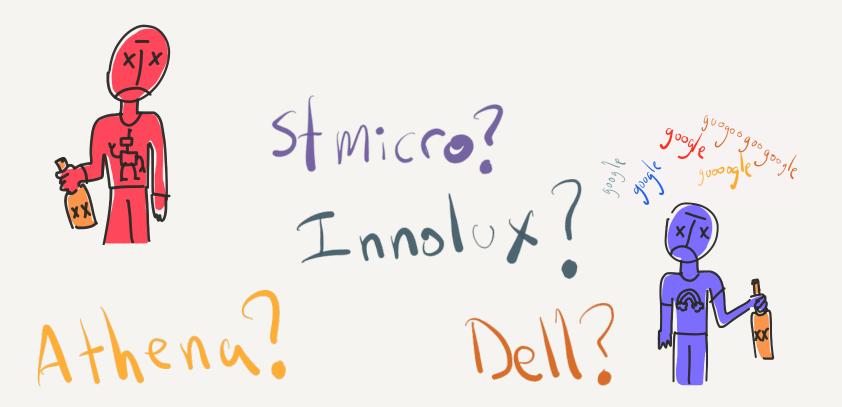


8/5/16

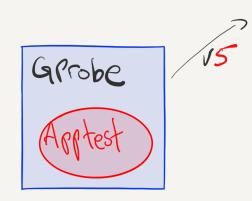


St Micro?











Genesis Microchip Technical Documentation

GProbe_User_Guide

5.2.1.15 RunCode

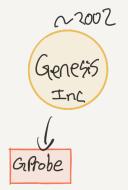
DEFCON24 A Monitor Darkly

1.5

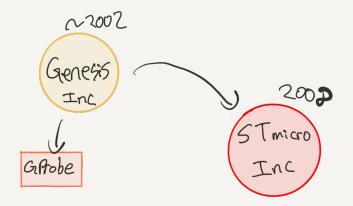




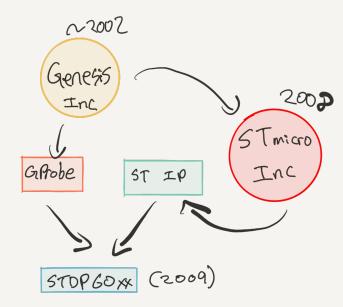




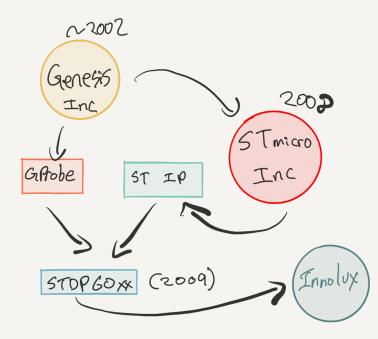




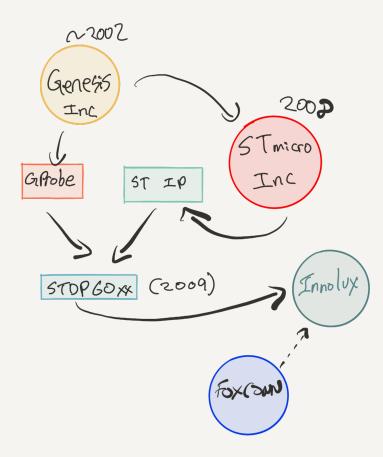




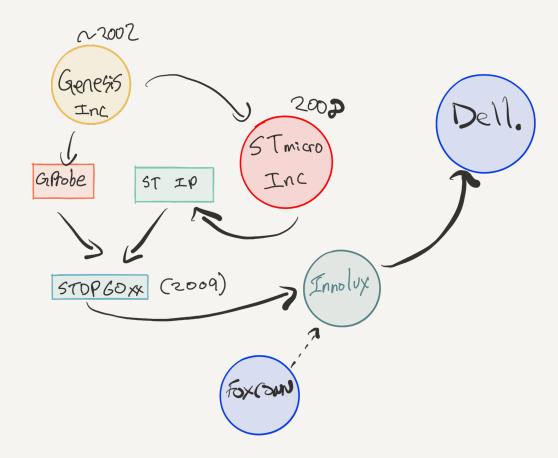














File View Register Terminal Commands Options Document Window Help	Genesis GProbe 5 - GProbe R			
Select Chip: FLI8638 Search: Filter: Image: Search: Search: Image: S	11		cument Windo	
Select Chip: Files: Description A Durent Saved S Search: File: Connection Settings X Description Address Value Size Connection Settings X Description E000 0 16 Description Select the type of device you wish to use GProbe to connect with. Device: Select the communication protocol. For the appropriate protocol version for your set-up, please consult GProbe documentation Protocol Select Select the communication tradies of protocol version for your set-up, please communication tradies of protocol version for your select Print messages from the board. Note that this option is only available for DDC2B Select Thint Enable Print Select Serial Connection for all Genesis Chips Se	🗅 🚅 🖬 % 🖻 🛍 0;	· 🛤 ┥ 🐷 🕐 🗙		↓↓ ✔ ♥ ★ ★ ○ ● 오 요 .
Search: Filter: Connection Settings Description Address Value Size Description Coorection Select the type of device you wish to use GProbe to connect with. Device: Select the communication protocol. For the appropriate protocol version for your set-up. please consult GProbe documentation Protocols Select Third Enable' if you wish to receive Print' messages from the bord on son your available for DDC2028				GProbe Register Document 1
Search: Filter: Image: Search: Search: Image: Search: Filter: Image: Search: Serial Image: Search: Search: Image: Search:<	Select Chip: FLI8638		-	Description A Current Saved S
Process Serial Parallel Description Address Value Size All E000 0 16 PRODUCT_ID E000 0 16 PRODUCT_REV E004 0 16 CLOCK_CONFIG1 E006 0 16 CLOCK_CONFIG2 E003 0 16 CLOCK_CONFIG3 E004 0 16 CLOCK_CONFIG3 E004 0 16 CLOCK_CONFIG3 E004 0 16 CLOCK_CONFIG3 E002 16 16 CLOCK_CONFIG3 E004 0 16 CLOCK_CONFIG3 E002 16 16 CLOCK_CONFIG3 E002 16 16 Commetter Select the communication protocol. For the appropriate protocol version for your set-up, please consult GProbe documentation Protocols Select the type of device you wish to receive Print' messages from the board. Note that this option is only available for DDC28I protocols and may cause communication traffic during sensitive chip operations. Enable Print Scheme Serial Connection for all Genesis Chips Serial Connection	Search:	Filter	Connec	tion Settings
Connection Serial Parallel Description Address Value Size HOST_CONTROL E000 0 16 HOST_CONFIGI E000 0 16 HOST_CLCK_CONFIGIS E000 0 16 HOST_CLCK_CONFIGIS E000 0 16 HOST_CLCK_CONFIGIS E000 0 16 HOST_CLCK_CONFIGIS E000 16 16 HOST_CLCK_CONFIGIS E000 16 16 HOST_CLCK_CONFIGIS E000 16 16 HOST_CLCK_CONFIGIS E000 <th></th> <th></th> <th>Pir</th> <th>Assignments USB Delays and Buffer Size</th>			Pir	Assignments USB Delays and Buffer Size
Description Address Value Size Image: Stript S				
Description Address Value Size Image: Stript S			-De	vices
With. PRODUCT_ID E000 0 16 PRODUCT_REV E004 0 16 CLOCK_CONFIG1 E006 0 16 CLOCK_CONFIG3 E00A 0 16 CLOCK_CONFIG3 E00A 0 16 CLOCK_CONFIG3 E00A 0 16 COCM_TCLK_DIV E00C 0 16 SOFT_RESETS E00E 0 16 COCM_TCLK_DIV E00C 0 16 COCM_TCLK_DIV E00C 0 16 COCM_TCLK_DIV E00C 16 Select 'Print Enable' if you wish to receive 'Print' messages from the board. Note that this option is only available for DDC28I protocols and may cause communication traffic during sensitive chip operations. Clock Enable Print Scheme Serial Connection for all Genesis Chips Serial Connection for all Genesis Chips Save As		Address Value	Size	
PRODUCT_ID E002 0 16 PRODUCT_REV E004 0 16 CLOCK_CONFIG1 E006 0 16 CLOCK_CONFIG2 E008 0 16 CLOCK_CONFIG3 E00A 0 16 CLOCK_CONFIG3 E00E 0 16 COM_TCLK_DIV E00C 0 16 CLOCK_CONFIG3 Sorterts Serial Select 'Print Enable' if you wish to receive 'Print' messages from the board. Note that this option is only available for DDC28! protocols and may cause communication traffic during sensitive chip operations. Enable Print Serial Connection for all Genesis Chips Save As Delete Save As </td <td></td> <td>E000 0</td> <td>wit</td> <td></td>		E000 0	wit	
PRODUCT_REV E004 0 16 CLOCK_CONFIG1 E006 0 16 CLOCK_CONFIG2 E008 0 16 CLOCK_CONFIG3 E00A 0 16			D.	wice:
CLOCK_CONFIG2 E008 0 16 CLOCK_CONFIG3 E00A 0	PRODUCT_REV			
Image: CLOCK_CONFIG3 E00A 0 16 Image: CLOCK_CONFIG3 E00A 0 16 Image: CLOCK_CONFIG3 E00C 16 16 Image: CLOCK_CONFIG3		Contraction and Contraction		tocols
OCM_TCLK_DIV E00C 0 16 SOFT_RESETS E00E 0 16 Registers Soripts Documents Batch Protocol: SERIAL1 Select 'Print' messages from the board. Note that this option is only available for DDC2BI protocols and may cause communication traffic during sensitive chip operations. Enable Print Scheme Serial Connection for all Genesis Chips Save As Delete			Jei	
Select 'Print Enable' if you wish to receive 'Print' messages from the board. Note that this option is only available for DDC2BI protocols and may cause communication traffic during sensitive chip operations. Enable Print Scheme Serial Connection for all Genesis Chips Save As Delete				sion for your service, please consult of robe documentation
Registers Scripts Documents Batch				tocol: SERIAL1
the board. Note that this option is only available for DDC2BI protocols and may cause communication traffic during sensitive chip operations. Enable Print Scheme Serial Connection for all Genesis Chips Save As Delete				ect 'Print Enable' if you wish to receive 'Print' messages from
Chip operations. Enable Print Scheme Serial Connection for all Genesis Chips Save As Delete	- Registers		the	board. Note that this option is only available for DDC2BI
Enable Print Scheme Serial Connection for all Genesis Chips Save As Delete	츼	-	A	
Scheme Serial Connection for all Genesis Chips			11	Enable Print
Serial Connection for all Genesis Chips				
Save As Delete			Sel	neme
			Se	rial Connection for all Genesis Chips 📃 📃
				Save As Delete
OK Cancel				
OK Cancel				
OK Cancel				
				OK Consul
				UK Cancel
		<u></u>		
Ready	Ready			
🏦 Start 🔢 🍘 🎆 🔍 🕲 🖌 🥝 🧼 🔢 🖉 Rahit 🕲 Ration 🖉 Global 🍘 LGEP 🗞 Genes 🛅 M	🔀 Start 🛛 😭 🥔 🖼 🗷		@Rohit	🕲 Ration 🖉 Global 🌾 LGEP 🗞 Genes 🔲 🕅

Connection Settings
Pin Assignments USB Delays and Buffer Size Connection Serial Parallel
Devices Select the type of device you wish to use GProbe to connect with.
Device: USB
Protocols
Select the communication protocol. For the appropriate protocol version for your set-up, please consult GProbe documentation
Protocol: DDC2Bi3b DDC2Bi3
Select 'Print Enable' if you wish to r DDC2Bi3a es from the board. Note that this option is DDC2Bi3b C2BI protocols and may cause communic DDC2Bi2 insitive chip operations. DDC2Bi1
Enable Print
Scheme
DDC2Bi Connection for Malibu (gm16xx) over USB-to-I2C 👤
Save As Delete
OK Cancel

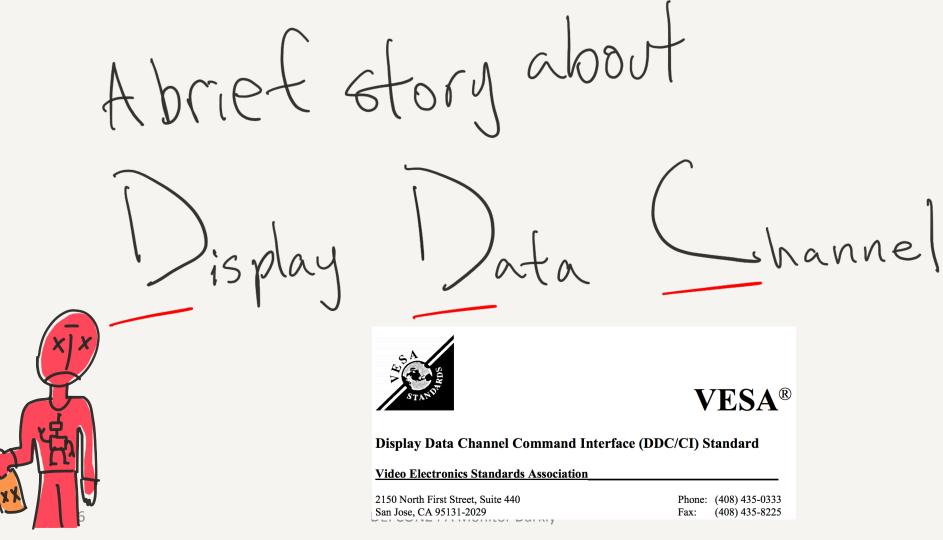
220 23.630423	1.2	nost	USBIIIS	40 SCSL. RESPONSE LON. 0X00 (CDB.C
221 23.856425	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00
222 23.856425	host	1.2	USB	539 URB_BULK out
223 24.028286	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (CDB:0
224 24.028286	host	1.2	USBMS	58 SCSI: Test Unit Ready LUN: 0x00
225 24.028286	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (Test
226 24.028286	host	1.2	USBMS	58 SCSI: Request Sense LUN: 0x00
227 24.043910	1.2	host	USB	45 URB_BULK in
228 24.043910	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (Reque
229 24.043910	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00
230 24.075157	1.2	host	USB	285 URB_BULK in
231 24.075157	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (CDB:0
232 24.996955	host	1.2	USBMS	58 SCSI: Test Unit Ready LUN: 0x00
233 24.996955	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (Test
234 24.996955	host	1.2	USBMS	58 SCSI: Request Sense LUN: 0x00
235 24.996955	1.2	host	USB	45 URB_BULK in
236 24.996955	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (Reque
237 25.121945	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00
239 25.137569	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (CDB:0
240 25.137569	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00
241 25.153192	1.2	host	USB	285 URB_BULK in
242 25.153192	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (CDB:0
243 25.153192	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00
244 25.153192	host	1.2	USB	539 URB_BULK out
245 25.387548	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (CDB:0
246 25.387548	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00
247 25.403172	1.2	host	USB	285 URB_BULK in
248 25.418795	1.2	host	USBMS	40 SCSI: Response LUN: 0x00 (CDB:€
249 25.965625	host	1.2	USBMS	58 SCSI Command: 0xcf LUN:0x00

USB Capture of Fu Update

Frame 238: 539 bytes on wire (4312 bits), 539 bytes captured (4312 bits)

	USBF	сар	ps	eud	lohe	ade	rι	engt	h :	27								
	IRP ID: 0xffffffffaa675998																	
	IRP USBD_STATUS: USBD_STATUS_SUCCESS (0x00000000)																	
	URB Function: URB FUNCTION BULK OR INTERRUPT TRANSFER (0x0009)																	
⊳	IRP	inf	orm	nati	on :	0x	00,	Dir	ect	ion	: F	DO	- >	PD0)			
	URB	bu s	id	1: 2														
	Devi	.ce	add	lres	s:	1												
0000	16	00	00	FO	67		<i>4</i> 4	ff	<i>4</i> 4	£ £	00	00	00	00	00	0	0	Va
0000																-	-	Yg
0010								00								-	-	n
0020	f9	51	86	c2	00	00	04	20	00	5f	CC	СC	CC	CC	СC	С	С	.Q
0030	CC	сс	сс	сс	сс	сс	сс	сс	сс	сс	сс	сс	сс	сс	сc	С	с	
0040	CC	сc	сс	сc	сc	сс	СC	СC	сc	сc	СC	сc	сc	СC	сc	С	С	
0050	CC	сc	сс	СC	СС	сс	СC	CC	СС	сс	СC	СС	СC	СC	СC	С	С	
0060	CC	сc	сс	сc	сс	сс	сс	CC	сс	сс	сc	сс	сс	сc	сc	C	С	
0070	CC	сc	сс	сc	сc	сс	СC	СC	сc	сс	СC	сc	сc	СC	сc	С	с	
0080	CC	сc	сс	СC	СС	сс	СC	CC	сс	сс	СC	сс	СC	СC	СC	С	С	
0090	CC	сс	сс	сc	сс	сс	сс	сc	сс	сс	сс	сс	сс	сс	сc	С	с	
¢																		





This table summarizes the DDC level upgrade requirements for both the Graphic Host and the Display Device.

From	То	Graphic Host H/W upgrade	Graphic Host S/W upgrade	Display Monitor H/W upgrade	Display Monitor S/W upgrade
DDC1	DDC2B	I ² C Bus Single Master (2 I/Os)	BIOS	I ² C Slave address A0/A1 support	DDC2B driver
DDC2B	DDC2Bi	No upgrade	DDC.DLL driver	6E/6F Slave address support	DDC2Bi driver (Simplified Access Bus)
DDC2B	DDC2B+	50/51 Slave address support	Access Bus Host driver (single device)	6E/6F Slave address support	Access Bus driver
DDC2B	DDC2AB	50/51 Slave address support	Access Bus Host driver (full spec)	6E/6F Slave address support	Access Bus driver

HTTP://CAXAPA.RU/THUMBS/349020/DDCCIV1.PDF

 JSB							
USB Mass Storage							
ScS-							
cno							
OxCF							

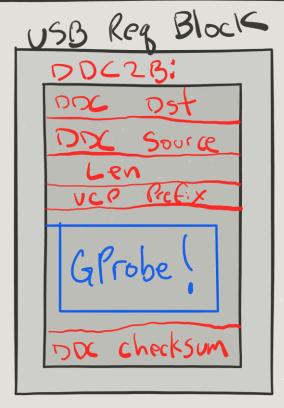
INITIATE COMMUNICATION OXCF = VENDOR SPECIFIC SCSICMD



24 A Monitor Darkly



8/5/16



ENCAPSULATED DOC2Bi PACKET

Sample Gibrobe Packet

RunCode

Request							
Name	Length	Value	Commen				
Length	1	Length of message + 1					
Command	1	0x1D					
Address	2						
Response							
ACK/NACK							





Packet from PC to Genesis chip								
Name	Length	Value	Comment					
DDC Destination	1	0x6E						
DDC Source	1	0x51						
Length	1	0x80 Length of VCP Prefix + Message	Length of VI P Protev +					
VCP Prefix	3	0xC2 0x00 0x00						
Message	variable							
Checksum	1	XOR of all previous bytes	byte chksum = 0; for (i = 0; i < buffer_size; ++i) chksum ^= buf[i];					

DDC2Bi PACKET & CHECKSUM ALGORITHM



USBM5/SCSI_reg(OxCF) USBORB/DDC2B; (Reg Read)

A SIMPLE REQUEST

USBM5/SCSI_reg(OxCF) USBORB/DDC2B; (Reg Read) USBMS/SCSI_Resp(OxCF)

A SIMPLE REQUEST

USBM5/SCSI_reg(OxCF) USBORB/DDC2B; (Reg Read) USBMS/SCSI_Resp(OxCF) USBMS/SCSI_REG (ORCF)

A SIMPLE REQUEST

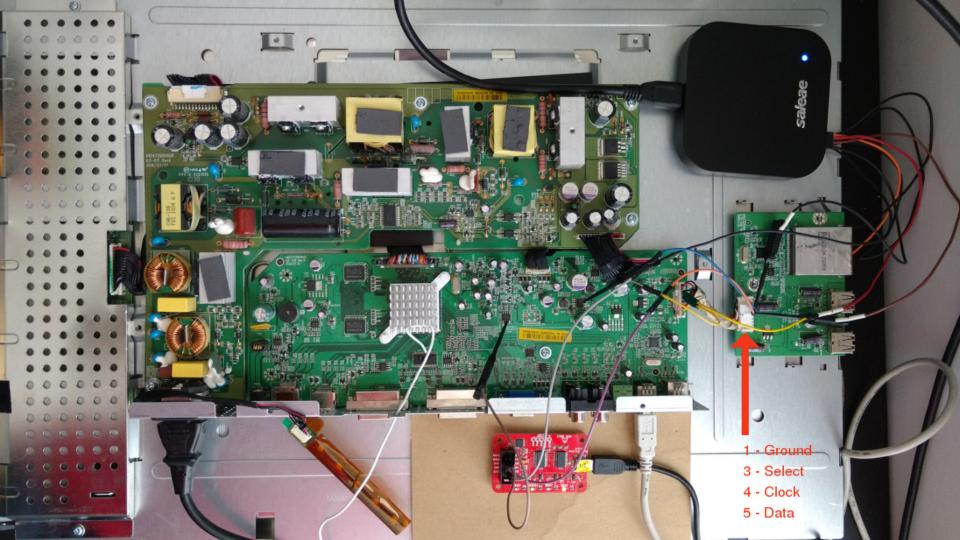
USBMS/SCSI_rea CoxCF) USBORB/DDC2B; (Reg Read) Send Command USBMS/SCSI_Resp(OxCF) USBMS/SCSI_REG (ORCF) USBURB/DD(ZBi (ACK) USBMS/SCST_Reg (OXCF)

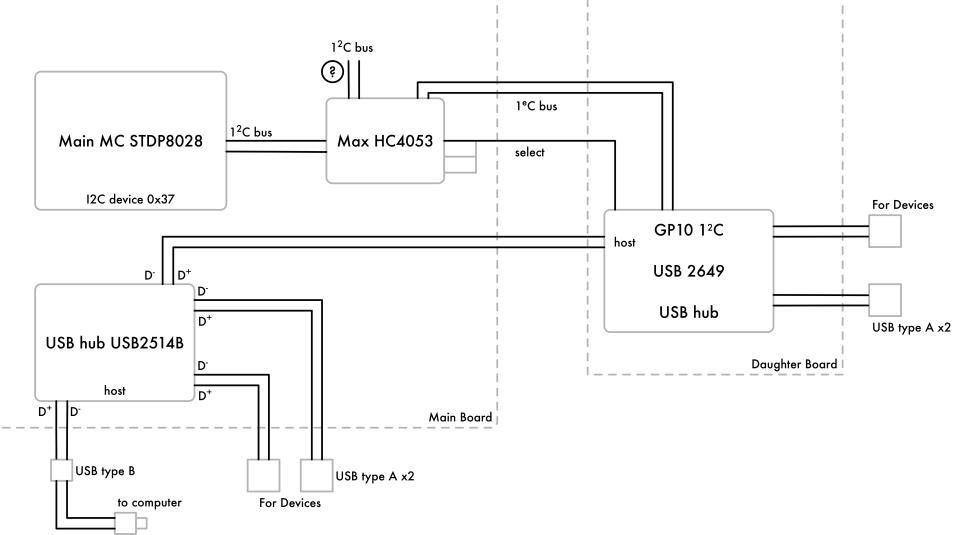
USBMS/SCSI_reg CoxCF) USBORB/DDC2B; (Reg Read) Send Command USBMS/SCSI_Resp(OxCF) USBMS/SCSI_REQ (ORCF) USBORB/DD(ZB; (Ack) (USBMS/SCS1_Reg (OXCF) USBM5/SCSI_reg(OxCF) USBORB/DDC2B; (Jet Royane)

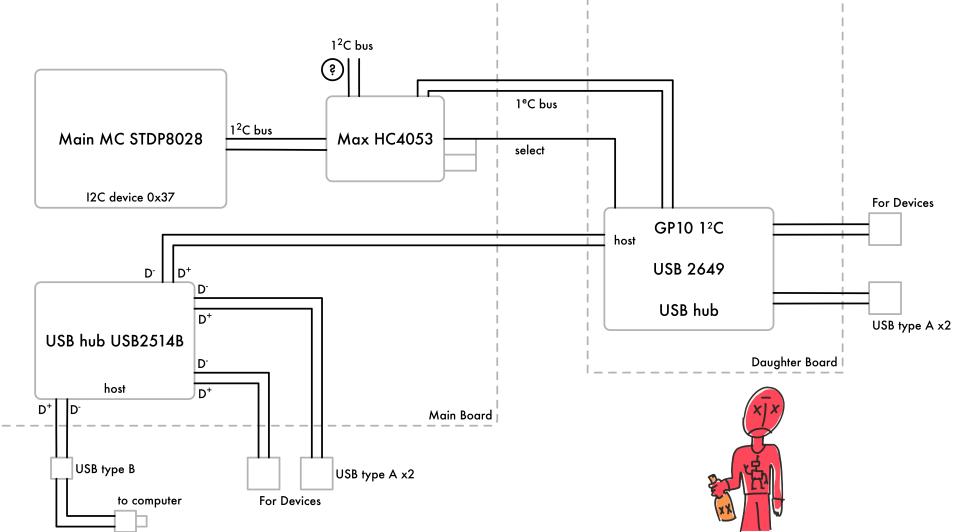
USBMS/SCSI_reg (oxCF) USBORB/DDC2B; (Reg Read) Send Command USBMS/SCSI_Resp(OxCF) USBMS/SCSI_REQ (ORCF) USBORB/DD(2B; (Ack) (USBMS/SCS1_Reg (OXCF) USBMS/SCSI_reg (OXCF) -USBORB/DDC2B; (Jet Royane) 45/SCSI_Resp(OxCF)

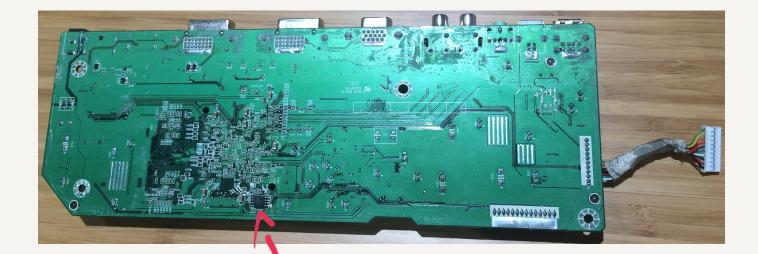












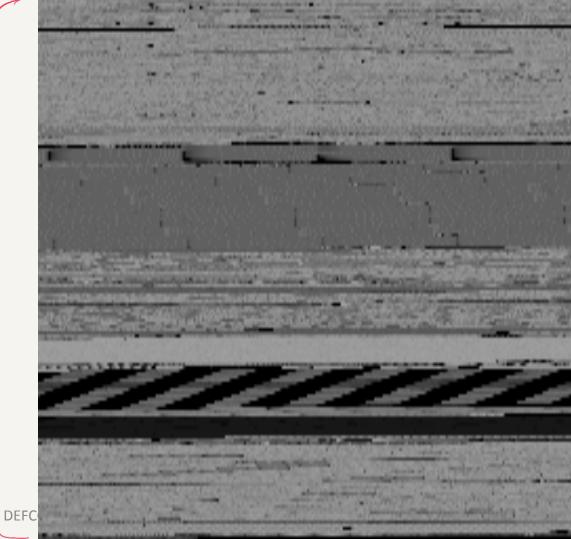
SPI Flash









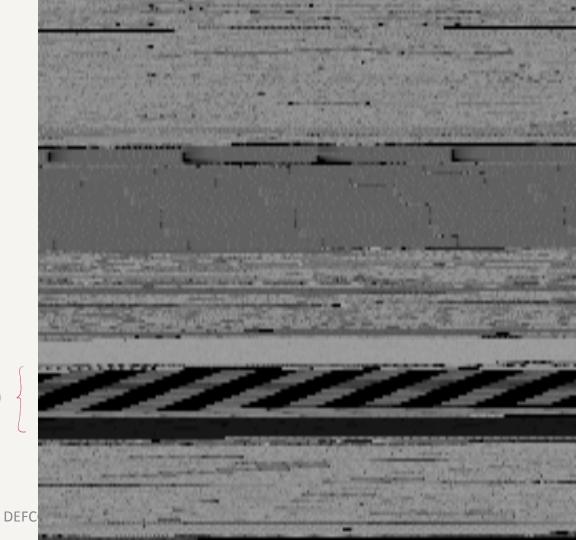


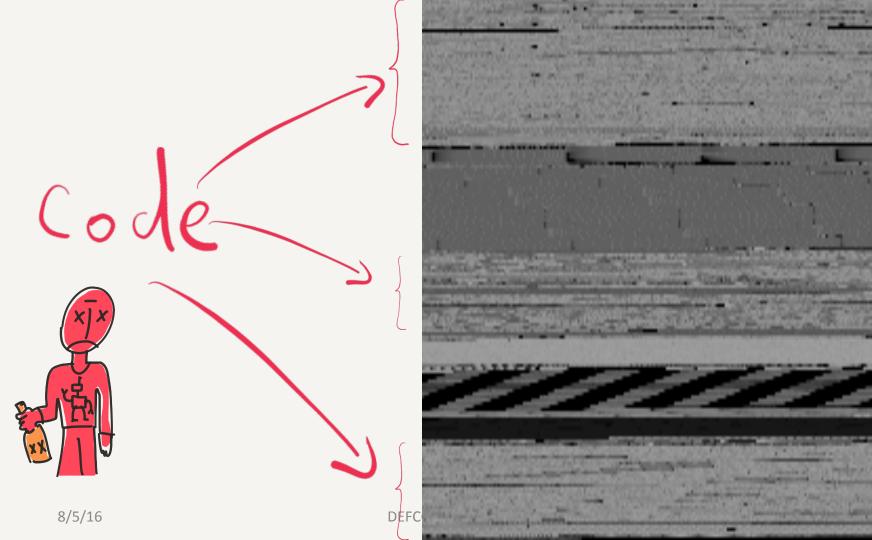
Avesome Sauce





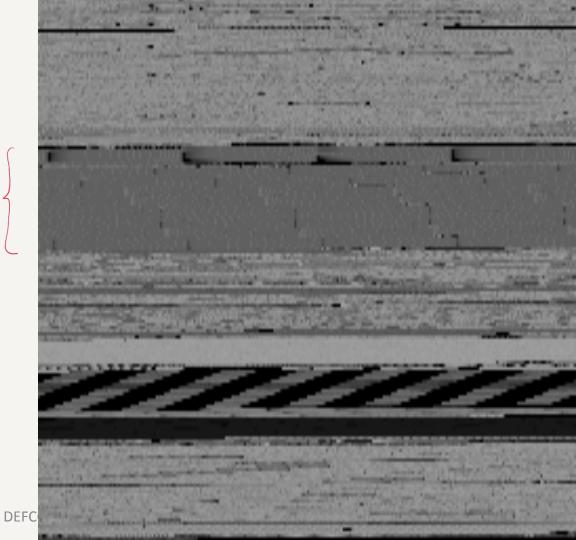


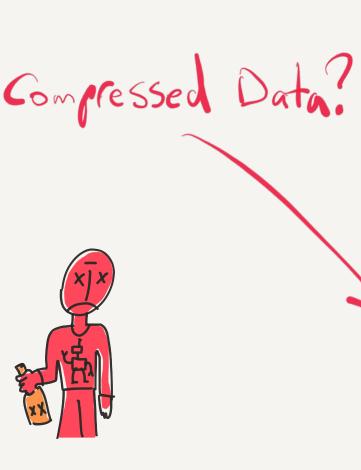


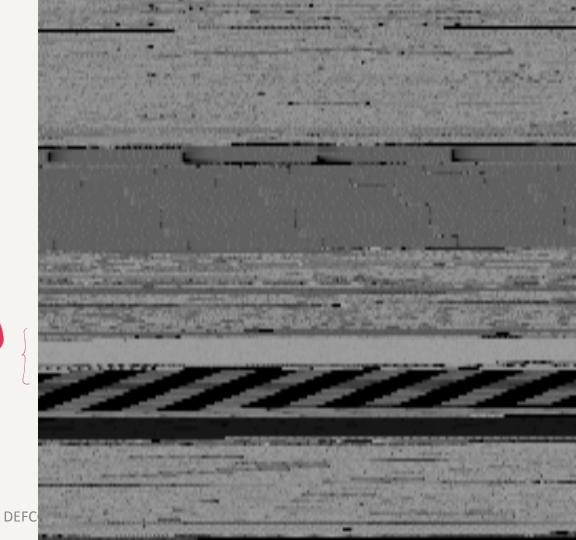












>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	>>>>update INNO)LUX	%d
 Innolux Mars Board			Change Input
DELL U2410			Appstest 52 0 Information
DELL2410 Code Ver -•			Appstest 52 2 for DVI1
			Appstest 52 3 for DVI2
Change Input -			Appstest 52 4 for DP
Appstest 50			Appstest 52 5 for HDMI
Appstest 50	2 Force swtich	ı to	Appstest 52 6 for Component Appstest 52 7 for CVBS
	3 Force swtich	1 to	
••			
	4 Force swtich	ιτο	
Appstest 50	5 Force swtich	ı to	Appstest 52 10 enter Factory mode appstest 57 1 : MTO_PIPMHide
chsksum=0x%x			appstest 57 2 : MTO_PIPMShow
Change Port Start	%d		appstest 57 3 : MTO_NoCable
Appstest 52 change s			appstest 57 4 : MTO_NoSync
			appstest 57 5 : MTO_OutOfRange
Appstest 52 change s	ource to DVI (HD	MIZ	appstest 57 6 : gm_OsdHide
Appstest 52 change s	ource to DVI (HD	MI3	appstest 57 7 : gm_OsdShow
Appstest 52 change s			Appstest 72 0 Display Information Appstest 72 1 x Adjust R1
Appstest 52 change s			Appstest 72 2 x Adjust R2
			Appstest 72 3 x Adjust R3
Appstest 52 change s			Appstest 72 4 x Adjust G1
A IA IA A LA A LA A LA A LA A LA A LA A			





xīx
PT IT
XX 8/5

			IC	0A - /Users/jatin/rbs/rbs_imgw3rx/dell_mor
: 📂 🔒 : 🗢 🗸 🔿 🗸 : 🏝 🦍 🦓	🌢 🖡 🖌	ā : 🔺 🥥	i 💼 💼 i	t 🛃 🖈 🐲 🖆 🗙 🤅 🕨 💷 🗌
Library function Data Regular		Unexplored	Instruction	
			IDA Vie	
	1	seg000:0000	; Input SHA256	: 5AC3E21BA2440D209B4AA2494374904C24352FA19
Function name				: 0C32B7A123F52383E756FD22DD77553F : 1C3A8743
<u></u> sub_86		seg000:0000 seg000:0000	; File Name :	/Users/jatin/rbs/rbs_imgw3rx/dell_monitor/
<u>f</u> nullsub_2			; Format : ; Base Address:	Binary file 0000h Range: 0000h - 200000h Loaded length
<u></u> sub_15D7		seg000:0000 seg000:0000		.686p
f sub_1617		seg000:0000 seg000:0000		.mmx .model flat
f sub_165F		seg000:0000 seg000:0000	; =========	
		seg000:0000 seg000:0000	; Segment type:	Pure code
		seg000:0000 seg000:0000	seg000	<pre>segment byte public 'CODE' use16 assume cs:seg000</pre>
📝 sub_1D8B		seg000:0000 seg000:0000	unk 0	assume es:nothing, ss:nothing, ds:nothing, db 0B8h ; \Leftrightarrow ; DATA XREF: seg00
<i>f</i> sub_1DBE		seg000:0001 seg000:0006	-	db 2 dup(0), 8Eh, 0D0h, 8Eh db 0D8h : • ; DATA XREF: sub /
<u>F</u> sub_25C5	•	seg000:0007 seg000:0007		db 8Eh, OCOh, OBCh, 0, 80h, OB8h, 2Ch, 0A9 ; DATA XREF: sub A
<i>f</i> sub_2869		seg000:0007 seg000:0014	unk 14	db OBEh, 2 dup(0) db OBFh; \Leftrightarrow ; DATA XREF: sub_1
f sub_2A12		seg000:0014 seg000:0015		db 0 ; sub_A728B+103↓r
<i>f</i> sub_2B6B	:	seg000:0016 seg000:0017		db 8
F sub_2C30	:	seg000:0018		db 0B9h ; db 52h ; R db 1Bh
f sub_2C73	:	seg000:0019 seg000:001A		db 2Bh ; +
₹ sub_2CCB	l i	seg000:001B seg000:001C		db OCFh ; db 0D1h ; db 0D1
		seg000:001D seg000:001E		db 0E9h ; db 0F3h ;
f sub_2D8C		seg000:001F seg000:0020		db 0A5h ; db 0B8h ;
<i>f</i> sub_2E1C		seg000:0021 seg000:0022		db 0 db 0
<i>f</i> sub_4029		seg000:0023 seg000:0024		db 8Eh ; 🚸 db 0D8h ; 🚸
f sub_43CB		seg000:0025 seg000:0026		db OFDh ; 🚸 dw 55B8h
<u>f</u> nullsub_3		seg000:0028 seg000:0029		db 55h ; U db 0BFh ; ∲
f sub_4EA3		seg000:002A seg000:002B		db 0 db 80h ; ∲
<i>f</i> sub_502E		seg000:002C seg000:002D		db 83h ; ∲ db 0EFh ; ∲
<i>f</i> sub_5030		seg000:002E seg000:002F		db 2 db 0B9h ; ∲
<i>f</i> sub_540A		seg000:0030 seg000:0031		db 0 db 4
	:	seg000:0032 seg000:0033		db 0F3h ; db 0ABh ;
		seg000:0034 seg000:0035		db OFCh ; db OBDh ;
<u>f</u> sub_6FB9	:	seg000:0036 seg000:0037		db 0 db 0
<u>f</u> sub_729A	•	seg000:0038	unk_38	db OEAh ;

March 31, 2008 07:54.27 CDT

April 11, 2008 21:10.13 CDT

Forums >> IDA Pro >> Embedded Code Reversing

Topic created on: March 29, 2008 18:46 CDT by memo5 2.

Hello All

OpenRCE

About

Articles

Book Store

Downloads

Forums

Search

Users

What's New

Customize Theme

blackgreen \$ set

Flag: Tornado! Hurricane!

Distributed RCE

Event Calendar

Live Discussion

Reference Library RSS Feeds ora

I'm working on reversing an embedded system, its my first attempt and need some advice, first of all the program file is in Intel-Hex format, so the code address is obtained by IDA, the target platform is x86 compatible, I'm facing some difficulties in setting the segments addresses and values cs,ds,es segments values. I appreciate any help.

igorsk 📶 🖂

What's the CPU? Is the code 16-bit or 32-bit? Is it the initial code (bootloader, BIOS) or is it something that's more high level? Are there datasheets available? Is the binary available for download somewhere or can you upload it?

In short, list as much info as you can and try to describe the actual problem you're having in more details. "Some difficulties" is not much to work with.

See also this.

nemo5 🔤 🖂

Ok igorsk thank you for your advice. And hope that this information will help.

The CPU Is Turbo186 the code is 16 bit.

The CPU run in extended mode using 24bit addressing capability. -The paragraph is not 16 byte its 256 byte so the CPU address space is 16MBand the EA calculated as: EA = (seament << 8) + offset.

The code is not just a Bootloader or BIOS it's the full firmware of a multimedia related control board. Unfortunately I can't upload the binary file, and it's not published any ware. The firmware mapped to address 0x60000, and the size of the firmware is 2MB

When I load the binary into IDA and disassemble the code I got code like this: seg000:6005CD push bp seg000:6005CE mov bp, sp seg000:6005D0 push si seg000:6005D1 mov si, [bp+6] seg000:6005D4 push si seg000:6005D5 call far ptr 6019h:0B1Fh --> Call 601900:0B1F seg000:6005DA pop cx seg000:6005DB cmp ax, 1 seq000:6005DE inz short near ptr 5E4h seg000:6005E0 xor ax, ax seg000:6005E2 jmp short near ptr 5EBh ---+ seg000:6005E4 --seq000:6005E4 push si <--+ seg000:6005E5 call far ptr 6306h:1Ch --> Call 630600:1C seg000:6005EA pop cx seq000:6005EB pop si <--+ seg000:6005EC pop bp seq000:6005ED retf You can notice that IDA could not recognize calls or jumps to near or far addresses.

To be specific how can I make IDA recognize the (24Bit) addressing mode, and correctly identify calls and jumps to other addresses?

igorsk 📶 🖂

April 12, 2008 20:58.17 CDT

I'm afraid it's not possible with current IDA version. The PC processor module is hardcoded to the standard x86 segmentation (ea = segment<<4 + offset). The best you can do is report this issue to lifak. This will probably need a new configuration flag in the processor module. In the meantime you could probably write a plugin or an IDC script which would walk through all the call instructions and fix the cross references.



\times 36 This game sucks...



· · · · · · · · · · · · · · · · · · ·		IDA - /03el3/jatil/iD3/iD3_illigw5l7/dell_illor
· 🚰 🔒 · ⇔▼ · 🏘 🚛 🦓	🏝 🖡 🔏 i 🗖 🌖 i 🎰	i 📾 🗗 🕏 🕈 🖆 🗙 i 🕨 🔲 🛄
Library function Data Regular	function Unexplored In	struction External symbol
F Functions window Image: Constraint of the second		IDA View-A So Hex View-1 Str
Function name		t SHA256 : 5AC3E21BA2440D209B4AA2494374904C24352FA190
	seg000:0000 ; Inpu seg000:0000	t CRC32 : 1C3A8743
f sub_86 f nullsub_2	seg000:0000 ; File seg000:0000 ; Form	
\vec{f} sub_15D7		Address: 0000h Range: 0000h - 200000h Loaded length
<i>f</i> sub_1617	seg000:0000 seg000:0000	.686p
<i>F</i> sub_165F	seg000:0000 seg000:0000	.model flat
f sub_16AB		
<i>F</i> sub_1A71		ent type: Fure code segment byte public 'CODE' use16
<i>f</i> sub_1D8B	seg000:0000 seg000:0000	assume cs:seg000 assume es:nothing, ss:nothing, ds:nothing,
	seg000:0000 unk_0 seg000:0001	db 0B8h ;
<u>f</u> sub_1DBE <u>f</u> sub_25C5	seg000:0006 unk_6 seg000:0007	db 0D8h ;
<i>f</i> sub_2869	seg000:0007 seg000:0007	; DATA XREF: sub_A2 db OBEh, 2 dup(0)
	<pre>seg000:0014 unk_14 seg000:0014</pre>	
<i>f</i> sub_2A12 <i>f</i> sub_2B6B	seg000:0015 seg000:0016	db 0 db 8
f sub_2C30	seg000:0017 seg000:0018	db 0B9h ; ∲ db 52h ; R
<i>f</i> sub_2C73	seg000:0019 seg000:001A	db 1Bh db 2Bh ; +
f sub_2CCB	seg000:001B seg000:001C	db OCFh : db OD1h :
f sub_2027	seg000:001D seg000:001E	db 0E9h ; ∲ db 0F3h ; ∲
f sub_2D8C	seg000:001F seg000:0020	db 0A5h ; ∲ db 0B8h ; ∲
f sub_2E1C	seg000:0021 seg000:0022	db 0 db 0
<i>f</i> sub_4029	seg000:0023 seg000:0024	db 8Eh ; ∲ db 0D8h ; ∲
<i>f</i> sub_43CB	seg000:0025 seg000:0026	db OFDh ; 🚸 dw 55B8h
f nullsub_3	seg000:0028 seg000:0029	db 55h ; U db 0BFh ; �
f sub_4EA3	seg000:002A seg000:002B	db 0 db 80h ; ∲
f sub_502E	seg000:002C seg000:002D	db 83h ; ↔ db 0EFh ; ↔
<i>f</i> sub_502E	seg000:002E seg000:002F	db 2 db 0B9h ; ∲
	seg000:0030 seg000:0031	db 0 db 4
f sub_540A	seg000:0032 seg000:0033	db OF3h ; db OABh ;
f sub_60FF	seg000:0034 seg000:0035	db OFCh ; db OBDh ;
f sub_6FB9	seg000:0036 seg000:0037	
<u>f</u> sub_729A	seg000:0038 unk_38	

IDA - /Users/jatin/rbs/rbs_imgw3rx/dell_mor

Computers are hard. Let'S ask Ilfak



	IDA - /Users/chris/Work/Dell_m1f1a_2	0160318124422.idb (D	ell_m1f1a.bin)				
: 📂 🔒 : 🖛 🗸 🛶 : 🐴 🦓 🐁 🏻 🎕	🔸 🔍 🖮 😓 📌 🕼 🛍 🛍 🔍 🗛 🖌	🛄 🔲 Remote GD	B debugger 🗘 🍖 🛃	: 🗊 🐏	*		
							0
Library function 📃 Data 🗧 Regular fu	unction 📕 Unexplored 📕 Instruction 📕 External symbol						
🖌 Functions window 🛛 🖸 🕲	IDA View-A, Hex View-1, Strings window	Structures	🕲 🖽 🛛 Enums 🛛 🕲 🍸	Imports	Exports	1	
Function name	DA View-A	000	O Hex View-1	000	Strings window		00
	AF3021 db 0Fh AF3022 ;		AF2E50 00 01 00 38 80 04 04 4 AF2E60 00 0F 30 10 08 02 04 0	1 F9 9F -	Address L	ength Typ	e Stri
	AF3022 push es AF3023 add ds1613h, ax AF3027 db 26h AF3027 push es		AF2ER0 88 48 44 E4 3F 22 01 3 AF2ER0 01 0A 65 24 F0 3C 04 2	0 80 00 (😒 seg054:A36 0	0000032 C	~~
	AF3027 push es		AF2E90 84 22 22 09 C9 F2 58 4 AF2EA0 FF 2A 42 11 A9 98 42 9		😒 seg054:A36 0	0000032 C	~~

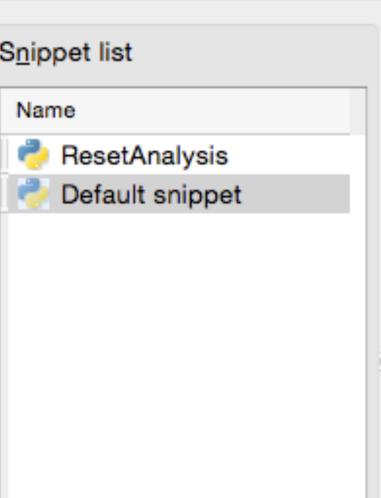






🕅 Execute script

Please enter script body



import idaapi def xjump(): ea = ScreenEA() da call = GetOpnd(ea, 0).sr for c in da call: if ":" in c: op op = op.split(':') seg = int(op[0][:-1], 16) off = int(op[1][:-1], 16) new ea = (seg * 0x100) +Jump(new ea) idaapi.CompileLine('static RunPythonStatement("xjump() 'py_x AddHotkey('Ctrl+Space',

RegRead

Request					
Name	Length	Value	Comment		
Length	1	Length of message + 1			
Command	1	0x06			
Register Address	2				
	Response				
Length	1	Length of message + 1			
Command	1	0x06			
Register Address	2				
Register Value	2				

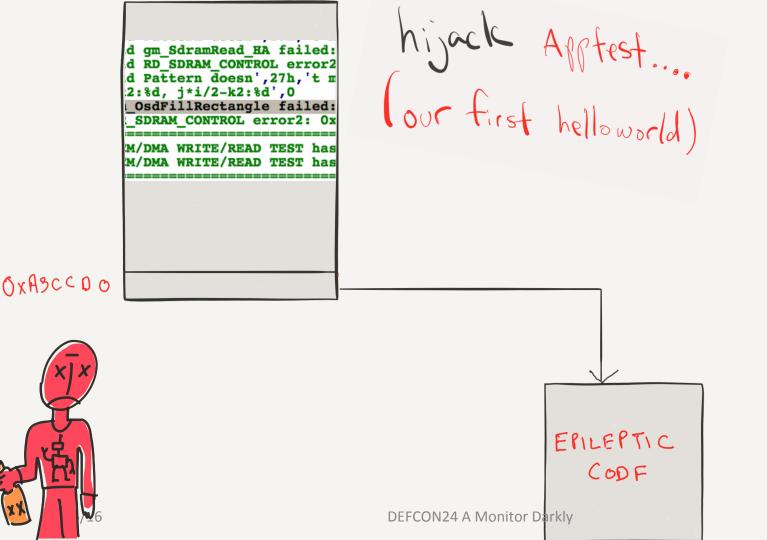
RunCode

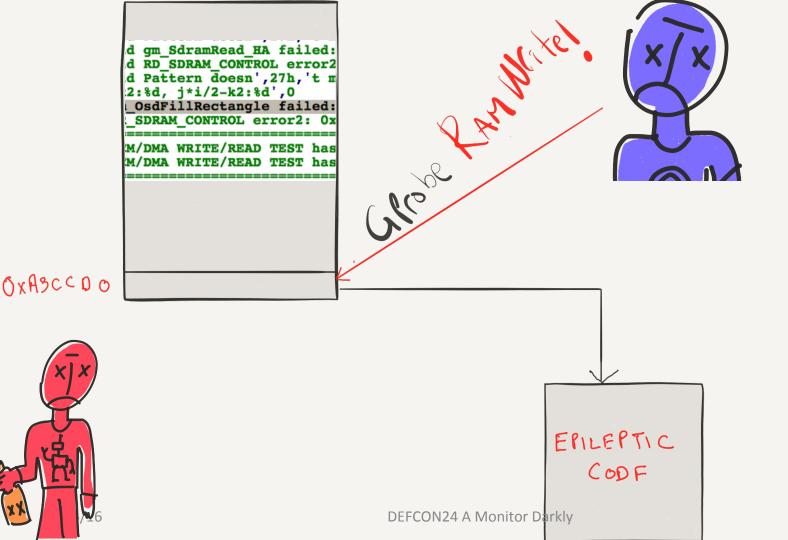
Request					
Name	Name Length Value Commen		Comment		
Length	1	Length of message + 1			
Command	1	0x1D			
Address	2				
Response					
ACK/NACK					

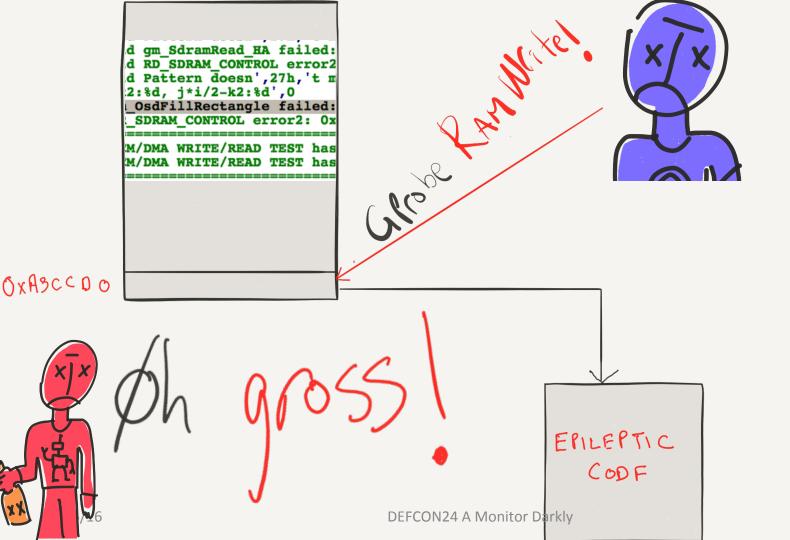
	RAM WRIT	E
	Request	
NAME	LEN	VALUE
Length	1	Message LEN 1
CMD	1	0 x 13
REG Address	2	
	Response	
Length	1	Message LEN 1
CMD	1	0 x 13
REG Address	2	
REG VAL	2	

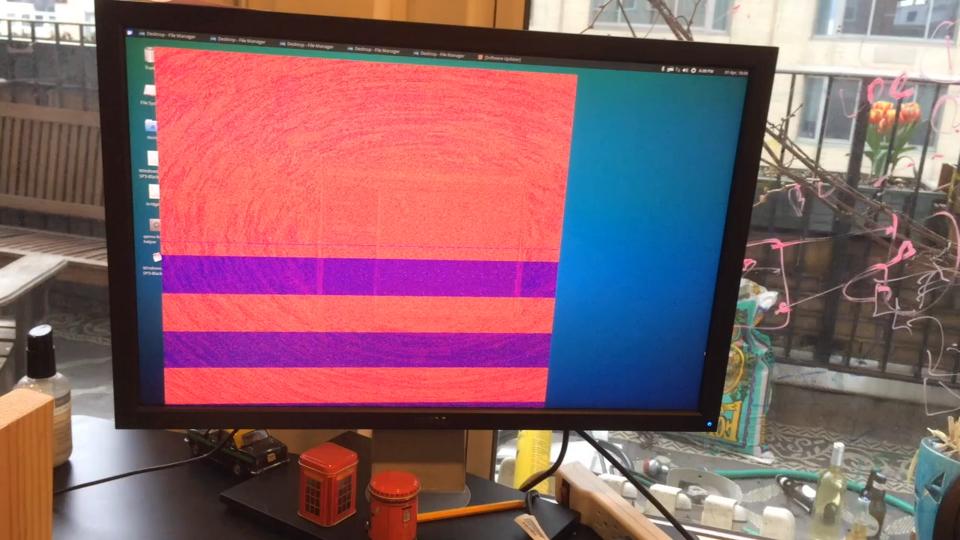
hijack Apptest.... lour first helloworld)











Monitor Memory world

"OSD Firmware"

 $\not > A \not > \phi \phi \phi \phi \phi$

8/5/

 $-\phi_{\mathsf{x}} \mathsf{B} \phi \phi \phi \phi$

	7D33		ax,	ax
:A71	7D35	push	ax	
:A71	7D36	push	CS	
:A71	FD37	mov	ax,	91h ; '�'
:A71	7D3A	push	ax	
:A71	D3B	call	far	ptr OF000h:252h ; print function!
:A71	FD40	add	sp,	6
:A71	FD43		ax,	
:A71	7D45	push	ax	
:A71	FD46	push	CS	
:A71	FD47	mov	ax,	OA3h ; '�'
:A71	FD4A	push	ax	
:A71	FD4B	call	far	ptr 0F000h:252h
:A71	rD50	add	sp,	6
/16 : A71	7D53	xor	ax,	
A71	7D55	nuch	a v	

Monitor Memory world

"OSD Firmware"

212225

ØXFØØØØØ

\$XA\$\$\$\$\$\$	φ×Βσφφφφ
------------------	----------

8/5/

A7FD33	xor ax, ax
A7FD35	push ax
A7FD36	push cs
A7FD37	mov ax, 91h; '�'
A7FD3A	push ax
A7FD3B	call far ptr OF000h:252h ; print function!
A7FD40	add sp, 6
A7FD43	xor ax, ax
A7FD45	push ax
A7FD46	push cs
A7FD47	mov ax, OA3h ; '�'
A7FD4A	push ax
A7FD4B	call far ptr OF000h:252h
A7FD50	add sp, 6
16 A7FD53	xor ax, ax
10 a7FD55	nuch av

Monitor Memory world

ØxFøøøøø

"OSD Firmware" $-\phi_{\mathsf{x}} \mathsf{B} \phi \phi \phi \phi$ PXADDDOD et 5 dump **DEFCON24 A Monitor Darkly**

Monitor Memory world

Firmware [[OSD ØxFøøøøø $-\phi_{\mathsf{x}} \mathsf{B} \phi \phi \phi \phi \phi$ PXADØØ60 USB LUMP XX

Monitor Memory world

Firmware [[OSD

 $-\phi_{\mathsf{x}} \mathsf{B} \phi \phi \phi \phi$ PXADØØØØ

ØxFøøøøø









Monitor Memory world

Firmware OSD

 $-\phi_{\mathsf{x}} \mathsf{B} \phi \phi \phi \phi \phi$ PXADDDOD

ØxFøøøøø

Durpoo

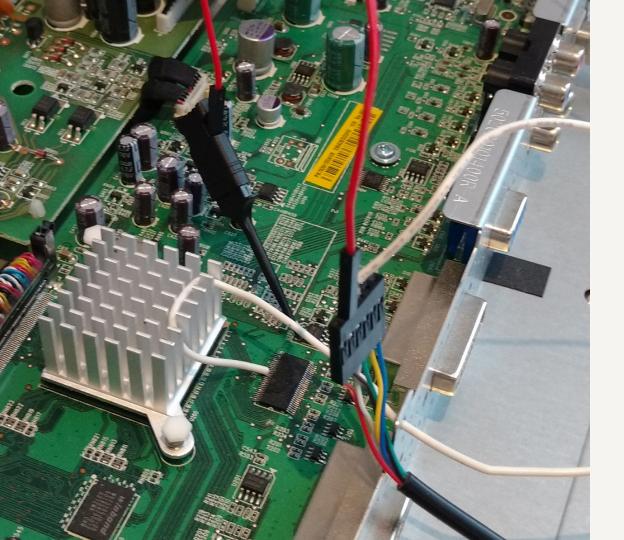


1) ump ...



Monitor Memory world







Welcome to minicom 2.7

OPTIONS: I18n Compiled on Sep 6 2015, 19:49:19. Port /dev/ttyUSB0, 17:29:46

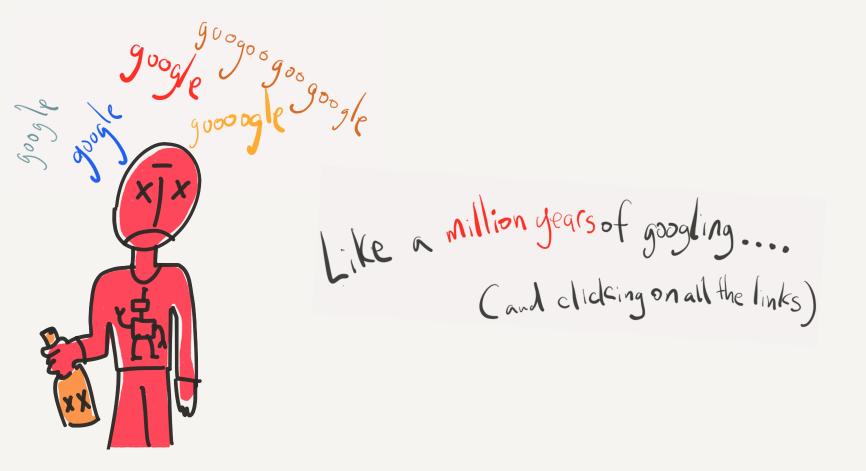
Press CTRL-A Z for help on special keys

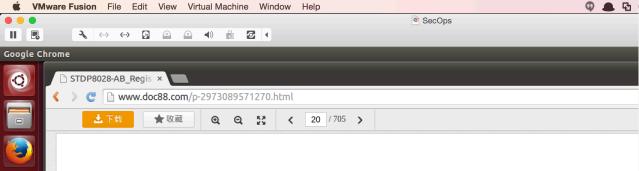
~~~ Exit MesInvState(Fly)~~~~ ~~~~Enter MesInvState(Fly)~~~~ ~~~ Exit MesInvState(Fly)~~~~ ~~~~Enter DefaultState~~~~ ~~~~Exit DefaultState~~~~ ~~~ Enter MesInvState(Fly)~~~~ ~~~ Exit MesInvState(Fly)~~~~ ~~~ Enter MesInvState(Fly)~~~~ ~~~ Exit MesInvState(Fly)~~~~ ~~~~Enter ValidMode\_StateState~~~~ ~~~~Exit ValidMode\_StateState~~~~ ~~~~Enter MesInvState(Fly)~~~~



Monitor Memory world

"05D Firmware ØxFøøøøø - \$x Bobbod ØXAØØØØØ IROM OCM Executable Con-chip Microcontroller) Sol Priver





OPEN IN A VM3

STDP8028-AB REGISTER LISTING

|       |          | 1 = TNR3 processing is disabled on left half of display output image. Normal TNR3 operation on right side of display. (Done by forcing motion value to max motion tnr coefficients) |
|-------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | Reserved | Reserved                                                                                                                                                                            |

# Reserved Register: 0xC818

>\_

Į

A

<mark>.a</mark>,

| 0xC81                           | A                | DP_RCAL_RESULT |                              |  |  |  |  |  |
|---------------------------------|------------------|----------------|------------------------------|--|--|--|--|--|
| POD: 0x00                       | 000              |                |                              |  |  |  |  |  |
| Display Port calibration Result |                  |                |                              |  |  |  |  |  |
| BIT                             | BIT NAME         |                | FUNCTION                     |  |  |  |  |  |
| 3:0                             | DPRX_RCAL_RESULT | DPRX Link C    | DPRX Link Calibration Result |  |  |  |  |  |
| 7:4                             | Reserved         | Reserved       | Reserved                     |  |  |  |  |  |
| 15:8                            | Reserved         | Reserved       |                              |  |  |  |  |  |

# 3.3.3 DISPLAY SIGNAL ADJUSTMENT FOR TTL PANEL SIGNALS AND OUTPUT CLOCKS

| 0xC81C    |                                                    | TIMING_CONFIG |                                                                                                                                                                                             |  | RW |  |  |  |  |
|-----------|----------------------------------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|----|--|--|--|--|
| POD: 0x00 | 000                                                |               |                                                                                                                                                                                             |  |    |  |  |  |  |
| Timing Co | Timing Configuration for Display and Audio Outputs |               |                                                                                                                                                                                             |  |    |  |  |  |  |
| BIT       |                                                    | BIT NAME      | FUNCTION                                                                                                                                                                                    |  |    |  |  |  |  |
| 0         | DCLK_I                                             | NV            | Invert DCLK pin                                                                                                                                                                             |  |    |  |  |  |  |
| 1         | DCLK_D                                             | DIS           | Disable DCLK output pin                                                                                                                                                                     |  |    |  |  |  |  |
| 2         | DCLK_F                                             | RATE_INV      | The transmitted display clock frequency at the oDCLK pad is 1x the internal pixel rate for<br>single wide TTL output, 1/2x the internal pixel rate for double wide TTL output, and 1/2x the |  |    |  |  |  |  |



Let's Display Picture! e -1-> EFCC Ionitor Darkly

where to transfer image

# www.dell.com

most be In The Firmware



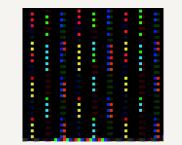
Darkly





|  |  | <br> |  |
|--|--|------|--|
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  | <br> |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |
|  |  |      |  |



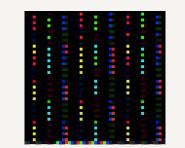






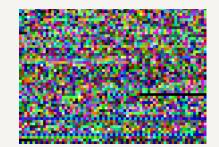


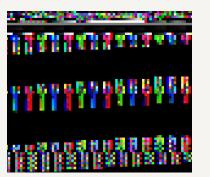




DEFCON24 A Monitor

But what about this?















E9 8F 2E C1 5D F7 11 5B 28 1C F7 CD B1 DB E5 96 0F 35 AE A9 D5 B0 50 DD FD 96 F3 6B 00 7C 6F C0 FF 92 ED 2A 7C 76 FF 43 87 47 83 1A 00 BE 47 77 95 0D B6 2F B4 33 4D 64 95 B4 11 3D 99 7F 36 C8 8D BD 8A A9 DD D8 7C BD 38 3F B2 FE E3 11 79 A8 69 D5 D9 88 59 A5 00 00 04 04 1D 03 78 00 78 00 58 03 40 01 72 03 1B 00 49 15 FB A8 0F 86 09 DB 41 F5 E4 4B 1A 2D 32 21 69 6B A5 EB E6 98 6F 75 55 9B 1A 12 97 54 C7 D4 32 8C 8F 62 B1 EC 99 FF CD 87 91 EF BB 40 1A E6 F1 00 1A EC 30 A0 E7 58 D4 69 56 EA E3 F8 98 7B 84 13 4E 7A AF E7 D7 79 60 B6 65 EF AC FA 90 9F F6 A0 37 AC 5D EE 86 A4 B5 02 4D 7B AC 24 3F D2 71 A9 EB 95 80 FF 00 00 00 00 00 00 00 00 00 00 00 03 00 84 D2 5D 6D 70 C2 83 E7 48 8A 5B B2 D5 05 27 61 90 73 D8 92 BE 5D 95 78 E1 03 EE 62 63 8A E6 32 BF 6D 84 68 CD E5 C0 92 00 F9 D3 13 B0 7C 37 B5 04 44 FB 5A 9B 07 80 97 A8 C6 DA 8C 58 9E 05 3F 34 6C 9F 6B 4D F6 EA 73 4B D2 A6 24 65 50 B1 AE D7 53 1F DE A6 AB 63 8D 30 C2 85 EF 4D E6 42 06 A0 74 C9 CB DC 2C C6 C3 4D 17 80 8D BF 20 B3 DE E0 51 00 FC D8 C7 A6 9A 20 9D CA 0B 12 FF E4 78 00 58 03 40 01 72 03 18 00 99 3E C2 91 48 C7 23 45 F9 52 C5 3C 58 7D AC FC F6 64 F6 3B 24 A0 D9 6A E4 1A B0 E7 4E 97 30 1C 4C A8 EA E8 B1 67 B7 BA 8F 17 1D 68 1D 8C CB 4E 86 30 3A F0 85 17 1A 71 32 2B BD A0 74 97 8B AE B0 9A 5A E5 14 77 4E 19 56 01 38 58 86 6E 2F 14 E7 E8 E9 C3 97 03 EE 28 98 5F 06 95 40 51 18 28 25 0A E6 44 43 4D 80 18 0D A2 6F 4F C0 82 00 00 00 00 00 00 00 00 00 00 00 7D F0 28 70 21 00 7C FD 7D F0 28 70 21 40 3C FD 75 F0 28 70 61 00 3C FC 7D F8 28 40 21 40 7C FC 7D F0 28 40 61 00 7C FC 7D F0 28 7D F0 28 40 21 40 7C FD 7D F0 28 70 21 00 7C FD 7D F8 28 70 21 00 7C FD 7D F8 28 70 21 00 7C FD 7D F0 28 60 21 00 7C FC 75 F0 28 70 21 00 7C 7D 7D F0 28 7D F4 28 70 21 00 3C 7D 7D F0 28 70 61 00 7C 7D 75 F0 28 70 21 00 3C FC 7D F0 28 70 61 40 7C FD 7D F0 28 60 21 40 3C FC 7D F0 28 7D F8 28 70 21 00 7C 7D 75 F8 28 60 61 00 3E FC 7D F0 28 70 21 00 7C FC 75 F0 28 70 21 00 3E FD 75 F0 28 70 61 00 7C FD 7D F8 28 7D F0 28 70 21 00 7C FC 7D F8 28 70 21 40 7C FD 7D F0 28 60 21 00 7C FD 7D F0 28 60 61 00 3C FD FD F0 28 60 21 00 7C FC 7D F8 28 7D F0 28 50 61 40 7C FC FD F8 28 60 21 00 3C 7D 7D F0 28 70 21 40 7C FD 7D F8 28 60 21 00 7C FD 7D F0 28 40 21 00 7C FD 7D F0 28 7D F0 28 60 21 00 3C FD 7D F0 2C 40 21 00 7D FD 7D F0 28 70 21 00 7C FC 7D F0 28 70 61 00 7C FC 7D F0 28 60 21 00 7C 7C 7D F0 28 7D F0 28 40 25 00 7C FD 75 F0 28 60 21 00 7C FD 7D F0 28 40 21 00 7C FD 75 F0 28 40 21 00 3E FC 7D F0 28 50 21 00 7C 7D F5 F0 28 7D F0 28 60 21 00 3E FC 7D F8 28 60 21 00 7C FC 7D F4 28 70 21 00 7C FD 7D F8 28 70 21 10 7C FD 7D F0 28 60 21 00 3C FC 7D F0 20 7D F0 28 40 21 00 7C FD 7D F0 28 70 21 00 3C FC 75 F0 28 40 21 10 7C FD 75 F0 28 60 21 00 7C FD 7D F0 2C 70 21 00 7C FD 7D F0 28 75 F4 28 68 21 00 3C FC 7D F0 2C 50 21 00 3C FD 7D F0 0E 00 00 7D



E9 8F 2E C1 5D F7 11 5B 28 1C F7 CD B1 DB E5 96 0F 35 AE A9 D5 B0 50 DD FD 96 F3 6B 00 7C 6F C0 FF 92 ED 2A 7C 76 FF 43 87 47 83 1A 00 BE 47 77 95 0D B6 2F B4 33 4D 64 95 B4 11 3D 99 7F 36 C8 8D BD 8A A9 DD D8 7C BD 38 3F B2 FE E3 11 79 A8 69 D5 D9 88 59 A5 00 00 04 04 1D 03 78 00 78 00 58 03 40 01 72 03 1B 00 49 15 FB A8 0F 86 09 DB 41 F5 E4 4B 1A 2D 32 21 69 6B A5 EB E6 98 6F 75 55 9B 1A 12 97 54 C7 D4 32 8C 8F 62 B1 EC 99 FF CD 87 91 FF BB 40 1A E6 F1 00 1A EC 30 A0 E7 58 D4 69 56 EA E3 F8 98 7B 84 13 4E 7A AF E7 D7 79 60 B6 65 EF AC FA 90 9F F6 A0 37 AC 5D EE 86 A4 B5 02 4D 7B AC 24 3F D2 71 A9 EB 95 80 FF 00 00 00 00 00 00 00 00 00 00 00 43 00 84 D2 5D 6D 70 C2 83 E7 48 8A 5B 82 D5 05 27 61 90 73 D8 92 BE 5D 95 78 E1 03 EE 62 63 8A E6 32 BE 6D 84 68 CD E5 C0 92 00 F9 D3 13 B0 7C 37 B5 04 44 FB 5A 9B 07 80 97 A8 C6 DA 8C 58 9E 05 3F 34 6C 9F 6B 4D F6 EA 73 4B D2 A6 24 65 50 B1 AE D7 53 1F DE A6 AB 63 8D 30 C2 85 EF 4D E6 42 06 A0 74 C9 CB DC 2C C6 C3 4D 17 80 8D BF 20 B3 DE E0 51 00 FC D8 C7 A6 9A 20 9D CA 0B 12 FF E4 78 00 58 03 40 01 72 03 18 00 99 3E C2 91 48 C7 23 45 F9 52 C5 3C 58 7D AC FC F6 64 F6 3B 24 A0 D9 6A E4 1A B0 E7 4E 97 30 1C 4C A8 EA E8 B1 67 B7 BA 8F 17 1D 68 1D 8C CB 4E 86 30 3A F0 85 17 1A 71 32 2B BD A0 74 97 8B AE B0 9A 5A E5 14 77 4E 19 56 01 38 58 86 6E 2F 14 E7 E8 E9 C3 97 03 EE 28 98 5F 06 95 40 51 18 28 25 0A E6 44 43 4D 80 18 0D A2 6F 4F C0 82 00 00 00 00 00 00 00 00 00 00 00 7D F0 28 70 21 00 7C FD 7D F0 28 70 21 40 3C FD 75 F0 28 70 61 00 3C FC 7D F8 28 40 21 40 7C FC 7D F0 28 40 61 00 7C FC 7D F0 28 7D F0 28 40 21 40 7C FD 7D F0 28 70 21 00 7C FD 7D F8 28 70 21 00 7C FD 7D F8 28 70 21 00 7C FD 7D F0 28 60 21 00 7C FC 75 F0 28 70 21 00 7C 7D 7D F0 28 7D F4 28 70 21 00 3C 7D 7D F0 28 70 61 00 7C 7D 75 F0 28 70 21 00 3C FC 7D F0 28 70 61 40 7C FD 7D F0 28 60 21 40 3C FC 7D F0 28 7D F8 28 70 21 00 7C 7D 75 F8 28 60 61 00 3E FC 7D F0 28 70 21 00 7C FC 75 F0 28 70 21 00 3E FD 75 F0 28 70 61 00 7C FD 7D F8 28 7D F0 28 70 21 00 7C FC 7D F8 28 70 21 40 7C FD 7D F0 28 60 21 00 7C FD 7D F0 28 60 61 00 3C FD FD F0 28 60 21 00 7C FC 7D F8 28 7D F0 28 50 61 40 7C FC FD F8 28 60 21 00 3C 7D 7D F0 28 70 21 40 7C FD 7D F8 28 60 21 00 7C FD 7D F0 28 40 21 00 7C FD 7D F0 28 7D F0 28 60 21 00 3C FD 7D F0 2C 40 21 00 7D FD 7D F0 28 70 21 00 7C FC 7D F0 28 70 61 00 7C FC 7D F0 28 60 21 00 7C 7C 7D F0 28 7D F0 28 40 25 00 7C FD 75 F0 28 60 21 00 7C FD 7D F0 28 40 21 00 7C FD 75 F0 28 40 21 00 3E FC 7D F0 28 50 21 00 7C 7D F5 F0 28 7D F0 28 60 21 00 3E FC 7D F8 28 60 21 00 7C FC 7D F4 28 70 21 00 7C FD 7D F8 28 70 21 10 7C FD 7D F0 28 60 21 00 3C FC 7D F0 2C 7D F0 28 40 21 00 7C FD 7D F0 28 70 21 00 3C FC 75 F0 28 40 21 10 7C FD 75 F0 28 60 21 00 7C FD 7D F0 2C 70 21 00 7C FD 7D F0 28 75 F4 28 68 21 00 3C FC 7D F0 2C 50 21 00 3C FD 7D F0 0E 00 00 7D

That's obviously the cond packet!

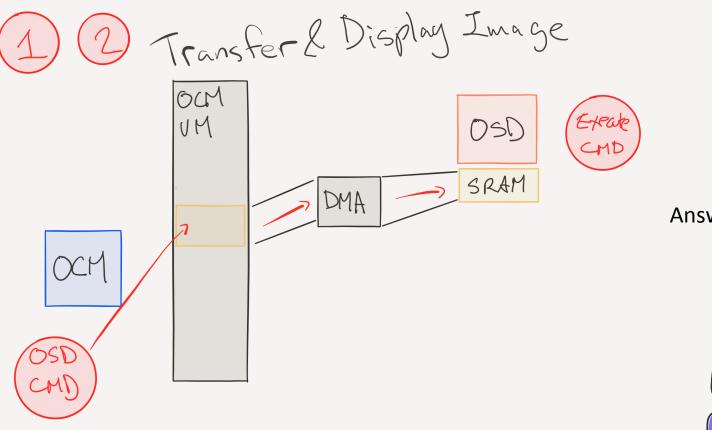


## OSD COMMAND CONTROL STRUCTURE

40 bytes in total

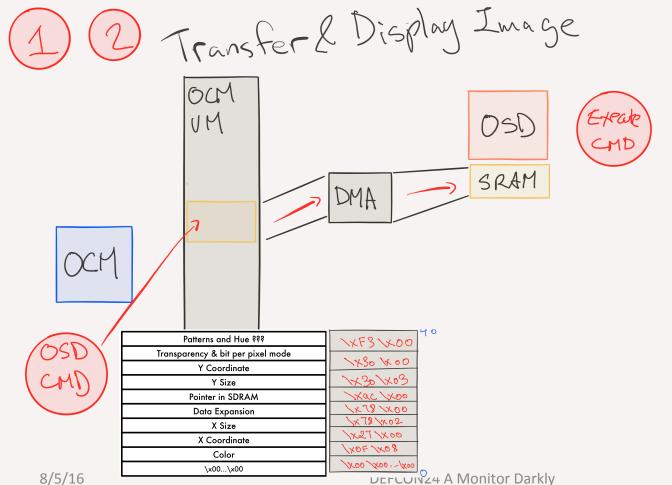
| Patterns and Hue ???              | 38 |  |  |  |  |  |  |  |
|-----------------------------------|----|--|--|--|--|--|--|--|
| Transparency & bit per pixel mode |    |  |  |  |  |  |  |  |
| Y Coordinate                      |    |  |  |  |  |  |  |  |
| Y Size                            |    |  |  |  |  |  |  |  |
| Pointer in SDRAM                  |    |  |  |  |  |  |  |  |
| Data Expansion                    |    |  |  |  |  |  |  |  |
| X Size                            |    |  |  |  |  |  |  |  |
| X Coordinate                      |    |  |  |  |  |  |  |  |
| Color                             |    |  |  |  |  |  |  |  |
| \x00\x00                          |    |  |  |  |  |  |  |  |





### Answered Question 1 & 2





#### Answered Question 1 & 2



8/5/16

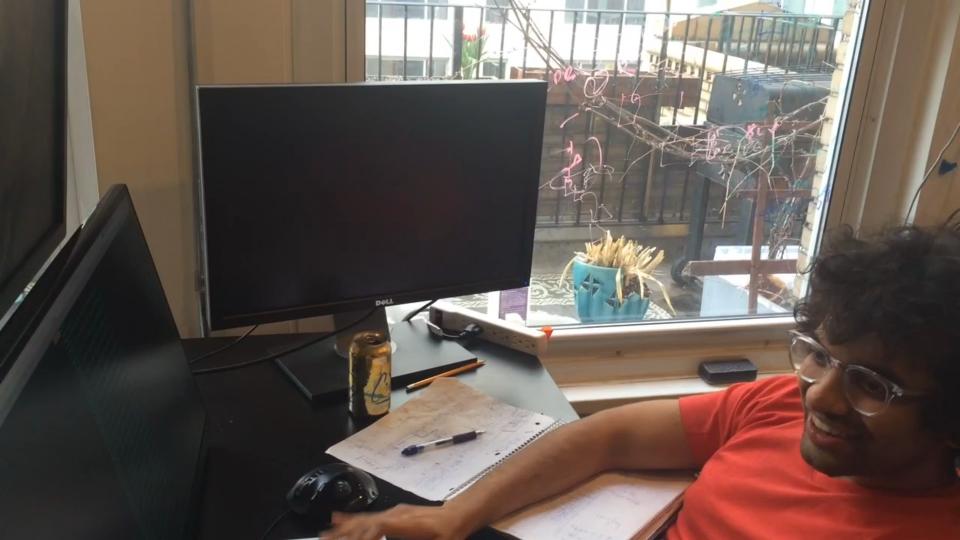
|                              | sdram_read_varia | ble_offs             | et proc              | far     |      |            | segF000:0  |               |        |                      |
|------------------------------|------------------|----------------------|----------------------|---------|------|------------|------------|---------------|--------|----------------------|
| segF000:7A12                 |                  |                      |                      |         | ; 80 | dram_read  | 0_rd_offs  | et+1Bip       |        |                      |
| segF000:7A12                 |                  |                      |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  | = word p             |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  | = word p             |                      |         |      |            |            |               |        |                      |
| segF000:7A12<br>segF000:7A12 |                  | = word p<br>= word p |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  | = word p             |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  | = word p             |                      |         |      |            |            |               |        |                      |
| seqF000:7A12                 |                  | = word p             |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  | = word p             |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  |                      |                      |         |      |            |            |               |        |                      |
| segF000:7A12                 |                  | push                 | bp                   |         |      |            |            |               |        |                      |
| segF000:7A13                 |                  |                      | bp, sp               |         |      |            |            |               |        |                      |
| segF000:7A15                 |                  | push                 | si                   |         |      |            |            |               |        |                      |
| segF000:7A16                 |                  |                      | di                   |         |      |            |            |               |        |                      |
| segF000:7A17                 |                  |                      | ds                   |         |      |            |            |               |        |                      |
| segF000:7A18                 |                  |                      | ax, 0                |         |      |            |            |               |        |                      |
| segF000:7A1B                 |                  |                      | ds, ax               |         |      |            |            |               |        |                      |
| segF000:7A1D                 |                  |                      | si, [bp+             |         | ; 41 | 15e        |            |               |        |                      |
| segF000:7A20                 |                  | cmp                  | [bp+arg_             |         |      |            |            |               |        |                      |
| segF000:7A24                 |                  | jz                   | short lo             |         |      |            |            |               |        |                      |
| segF000:7A26                 |                  | cmp                  | [bp+arg_             |         |      |            |            |               |        |                      |
| segF000:7A2A<br>segF000:7A2C |                  | jz                   | short lo             |         |      |            |            |               |        |                      |
| seqF000:7A30                 |                  | jz                   | [bp+arg_<br>short lo |         |      |            |            |               |        |                      |
| seqF000:7A32                 |                  | test                 | [bp+arg              |         |      |            |            |               |        |                      |
| seqF000:7A37                 |                  | jz                   | short lo             |         |      |            |            |               |        |                      |
| segF000:7A39                 |                  | -                    |                      |         |      |            |            |               |        | Transfors the images |
| segF000:7A39                 | loc 7A39:        |                      |                      |         | ; 00 | ODE XREF:  | sdram rea  | d variable of | ffset+ | Transfers the image  |
| segF000:7A39                 |                  |                      |                      |         |      |            |            | offset+18 j   |        | 0                    |
| segF000:7A39                 |                  | mov                  | ax, 4                |         |      |            |            |               |        |                      |
| segF000:7A3C                 |                  | jmp                  | loc_7B2D             | 1       |      |            |            |               |        |                      |
| segF000:7A3F                 | ;                |                      |                      |         |      |            |            |               |        |                      |
| segF000:7A3F                 |                  |                      |                      |         |      |            |            |               |        |                      |
| segF000:7A3F                 | loc_7A3F:        |                      |                      |         | ; 0  | ODE XREF:  | sdram_rea  | d_variable_of | ffset+ | •                    |
| segF000:7A3F                 |                  | mov                  | ax, [bp+             | arg_6]  |      |            |            |               |        |                      |
| segF000:7A42                 |                  |                      | ax, 1                |         |      |            |            |               |        |                      |
| segF000:7A44                 |                  | imul                 | [bp+arg_             | 8]      |      | -20        |            |               |        |                      |
| segF000:7A47<br>segF000:7A49 |                  |                      | di, ax               |         | ; 0: | ¥20        |            |               |        |                      |
| seqF000:7A49                 |                  | call                 | cs<br>near ptr       | aub 762 | 7    |            |            |               |        |                      |
| segF000:7A4D                 |                  | push                 | [bp+arg              |         |      |            |            |               |        |                      |
| seqF000:7A50                 |                  | push                 | [bp+arg              |         |      |            |            |               |        |                      |
| seqF000:7A53                 |                  | push                 | [bp+arg              |         |      |            |            |               |        |                      |
| segF000:7A56                 |                  | push                 | [bp+arg_             |         |      |            |            |               |        |                      |
| segF000:7A59                 |                  | push                 | [bp+arg              |         |      |            |            |               |        |                      |
| segF000:7A5C                 |                  | push                 | [bp+arg              |         |      |            |            |               |        |                      |
| segF000:7A5F                 |                  |                      |                      |         | 221  | E+2 ; 76c) | 1          |               |        |                      |
| segF000:7A63                 |                  |                      | sp, OCh              |         | _    |            |            |               |        |                      |
| segF000:7A66                 |                  |                      |                      | ds:loc_ | D3E1 | 1+1, 1 ; ; | start sdra | m read        |        |                      |
| segF000:7A6B                 |                  | mov                  | es, [bp+             |         | ; 41 | 15e        |            |               | У      | 7                    |
| segF000:7A6E                 |                  | jmp                  | short lo             | C_7AB3  |      |            |            |               |        |                      |

| seqF000:77F0                 |                  |              |           |        |        |     |                                             |
|------------------------------|------------------|--------------|-----------|--------|--------|-----|---------------------------------------------|
|                              | sdram write var. | iable of     | feat      | nroc   | far    |     | CODE XREF: segF000:loc DElj                 |
| seqF000:77F0                 | wille var.       | Table_01     | 2000      | proc   |        | '   | Sona anari begroovitoo_baij                 |
| seqF000:77F0                 | arg 0            | = word       | ptr       | 6      |        |     |                                             |
| segF000:77F0                 |                  | = word       |           | ă.     |        |     |                                             |
| segF000:77F0                 |                  | = word       |           | OAh    |        |     |                                             |
| segF000:77F0                 |                  | = word       |           | OCh    |        |     |                                             |
| segF000:77F0                 |                  | = word       |           | OEh    |        |     |                                             |
| segF000:77F0                 |                  | = word       |           | 10h    |        |     |                                             |
| segF000:77F0                 | arg_C            | = word       | ptr       | 12h    |        |     |                                             |
| segF000:77F0                 | arg_E            | = word       | ptr       | 14h    |        |     |                                             |
| segF000:77F0                 | arg_10           | = word       | ptr       | 16h    |        |     |                                             |
| segF000:77F0                 |                  | = word       |           | 18h    |        |     |                                             |
| segF000:77F0                 |                  | = byte       |           | 1Ah    |        |     |                                             |
| segF000:77F0                 | arg_16           | = word       | ptr       | 1Ch    |        |     |                                             |
| segF000:77F0                 |                  |              |           |        |        |     |                                             |
| segF000:77F0                 |                  | push         | bp        |        |        |     |                                             |
| segF000:77F1                 |                  | mov<br>push  | bp,<br>si | sp     |        |     |                                             |
| segF000:77F3<br>segF000:77F4 |                  | push         | di        |        |        |     |                                             |
| seqF000:77F5                 |                  | push         | ds        |        |        |     |                                             |
| segF000:77F6                 |                  | mov          | ax,       | 0      |        |     |                                             |
| segF000:77F9                 |                  | mov          | ds,       |        |        |     |                                             |
| seqF000:77FB                 |                  | mov          |           | [bp+a  | rg Cl  |     | buffer                                      |
| seqF000:77FE                 |                  | cmp          |           | arg_4  |        | 1   |                                             |
| seqF000:7802                 |                  | jz           |           |        | 783A   |     |                                             |
| segF000:7804                 |                  | cmp          |           | arg_6  |        |     |                                             |
| segF000:7808                 |                  | iz           |           | rt loc |        |     |                                             |
| segF000:780A                 |                  | cmp          |           | arg_8  |        |     |                                             |
| segF000:780E                 |                  | jz           |           | rt loc |        |     |                                             |
| segF000:7810                 |                  | cmp          |           | arg_1  |        |     |                                             |
| segF000:7814                 |                  | jz           | shor      | rt loc | _783A  |     |                                             |
| segF000:7816                 |                  | mov          |           |        | rg_10] |     |                                             |
| segF000:7819                 |                  | or           |           |        | rg_12] |     |                                             |
| segF000:781C                 |                  | jz           |           |        | _7840  |     |                                             |
| segF000:781E                 |                  | mov          | al,       | [bp+a  | rg_14] |     |                                             |
| segF000:7821                 |                  | cpM          |           |        |        |     |                                             |
| segF000:7822                 |                  | and          | ax,       |        | 151    |     |                                             |
| segF000:7825                 |                  | cmp          |           | 60h ,  |        |     |                                             |
| segF000:7828                 |                  | jl<br>push   |           | rt loc |        |     |                                             |
| segF000:782A<br>segF000:782D |                  | push         |           | arg_1  |        |     |                                             |
| segF000:7830                 |                  | call         |           | 775B   |        |     | checking bounds with 0x7FFF                 |
| seqF000:7833                 |                  | add          | sp,       |        |        | 1   | chocking bounds with oxirir                 |
| segF000:7836                 |                  | or           | ax,       |        |        |     |                                             |
| segF000:7838                 |                  | inz          |           | rt loc | 7840   |     |                                             |
| segF000:783A                 |                  |              |           |        |        |     |                                             |
| segF000:783A                 | loc 783A:        |              |           |        |        | ;   | CODE XREF: sdram_write_variable_offset+12 j |
| segF000:783A                 |                  |              |           |        |        |     | sdram_write_variable_offset+18 j            |
| segF000:783A                 |                  | mov          | ax,       | 4      |        |     |                                             |
| segF000:783D                 |                  | jmp          |           | 79DD   |        |     |                                             |
| segF000:7840                 | ;                |              |           |        |        |     |                                             |
| segF000:7840                 |                  |              |           |        |        |     |                                             |
| segF000:7840                 | loc_7840:        |              |           |        |        |     | CODE XREF: sdram_write_variable_offset+2Clj |
| segF000:7840                 |                  |              |           |        |        | ;   | <pre>sdram_write_variable_offset+381j</pre> |
| segF000:7840                 |                  | push         | CB        |        |        |     |                                             |
| segF000:7841                 |                  | call         |           |        | sub_75 | БZ  |                                             |
| segF000:7844                 |                  | push         |           | arg_A  |        |     |                                             |
| segF000:7847                 |                  | push         |           | arg_8  |        |     |                                             |
| segF000:784A<br>segF000:784D |                  | push<br>push |           | arg_6  |        |     |                                             |
| seqF000:7850                 |                  | push         |           | arg_a  |        |     |                                             |
| segF000:7853                 |                  | push         |           | arg 0  |        |     |                                             |
| segF000:7856                 |                  | call         |           |        |        | c 2 | 22B+1 ; 7686                                |
| segF000:785A                 |                  | add          | sp,       |        |        | -   |                                             |
| seqF000:785D                 |                  | mov          |           |        | rg_10] |     |                                             |
| segF000:7860                 |                  | or           |           |        | rg_12] |     |                                             |
| segF000:7863                 |                  | jnz          |           |        | 78DC   |     | L                                           |
|                              |                  | mov          |           |        | rg 16] |     | r                                           |
| segF000:7865                 |                  |              |           |        |        |     |                                             |
| segF000:7865<br>segF000:7868 |                  | mul          |           | arg 8  |        |     |                                             |

Transfers the image



A Monitor Darkly



... what is a color





Box with

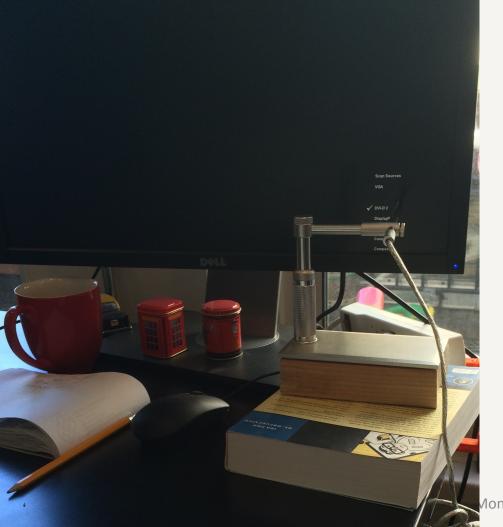
Color 0 Color 1 Color 2 Color 3



arkly

Science Time!



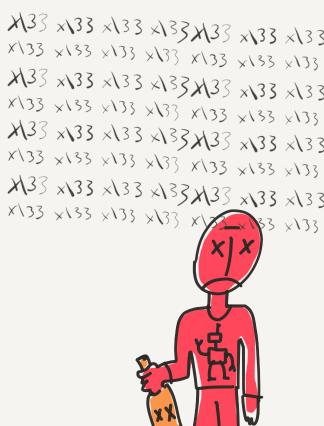


Science Time!



**Nonitor Darkly** 



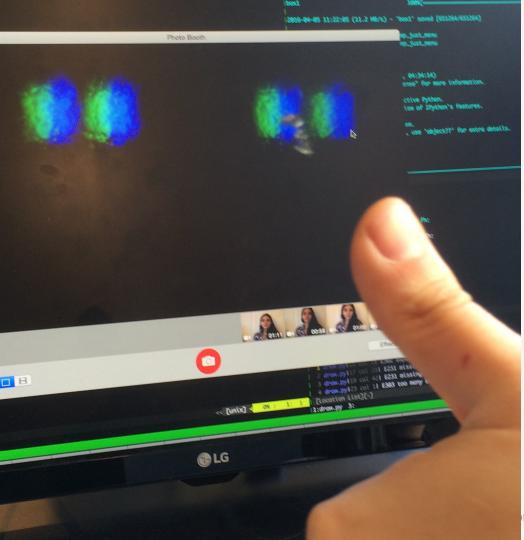




×\33 ×\ØØ ×\33 ×\ØØ



r Darkly



×\33 ×\ØØ ×\33 ×\ØØ

How Many Bits Per Pixel?

r Darkly

4 bits per pixel?





4 bits per pixel? How do you encode a COLOR with 4 bits?



# 8 bit 8 bit 8 bit 8 bit 8 bit 8 bit

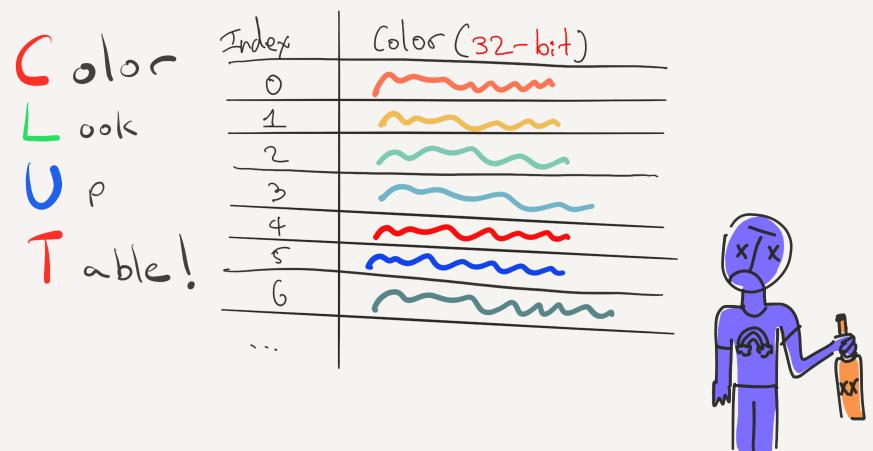


# 1 bit 1 bit 1 bit



Color Look Up Table!





here is the CLUT

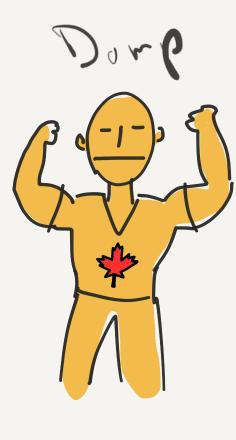












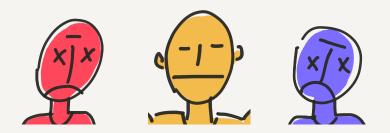


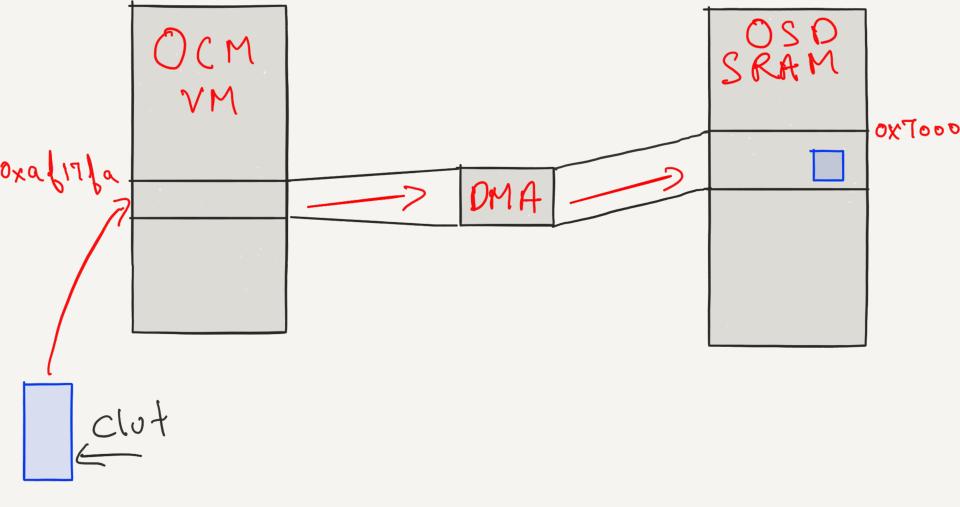


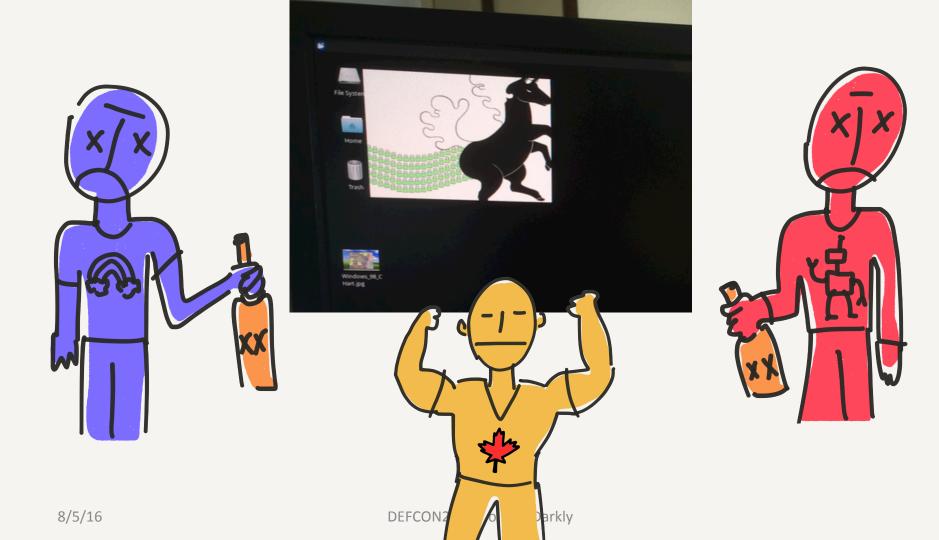


Ke Z days hater

oh look at that









#1++? huh?



## 4.16 OSD

The gm1601 has a fully programmable, true color bitmapped OSD controller capable of displaying up to 12 "tiles" or bitmap windows on the display. The individual tiles are programmable for location, size, and bits per pixel, and have a precedence determining which tiles appear when overlapping occurs on the display. Tile data is stored in the external framestore memory by the system controller in either: 1, 2, 4, or 8 bit per pixel format. On-chip table registers point to the start of tiles in external memory. Two programmable on-chip 256 x 24-bit color lookup tables are provided to map the OSD pixels onto a true 24 bit color space using the first table for one mapping, and the second table for an alternate mapping.



#### VMware Fusion File Edit View Virtual Machine Window Help

#### 

#### Google Chrome

🗅 S

| STDP80 | 28-AB_Regis ×             |           |                       |       |
|--------|---------------------------|-----------|-----------------------|-------|
| C      | www.doc88.com/p-297308957 | 1270.html |                       |       |
| 2      | 、下载 ★收藏 Q Q               | 53 K      | 392 / 705 <b>&gt;</b> |       |
|        |                           |           |                       | Demon |

#### 3.25 OCM BREAKPOINTS AND CODE-PATCH

These are 4 sets of registers for use in debug and patching of OCM mask-rom code. The OCM address for any memory access (code read, or data r/w) is compared, with a selectable mask of the low bits, to a "breakpoint" address. When the OCM address matches, either an BP\_IRQ may be generated or the OCM addr ess will be substituted with a new address to "redirect" the OCM to a different part of the RAM or ROM (and patch over code bugs, or change ROM data tables). The BP\_IRQ is available as an interrupt source to OCM\_IRQ0 of the on chip microprocessor.

SecOps

🔺 🔁



| 0xD7C0                        |        | BP0_C    | BP0_CTRL                                                                                                                                                                                     |                                                                                                                                                                                                                                            |                       |  |
|-------------------------------|--------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|--|
| POD: 0x0000                   |        |          |                                                                                                                                                                                              |                                                                                                                                                                                                                                            |                       |  |
| Firmware Breakpoint 0 Control |        |          |                                                                                                                                                                                              |                                                                                                                                                                                                                                            |                       |  |
| BIT                           |        | BIT NAME |                                                                                                                                                                                              | FUNCTION                                                                                                                                                                                                                                   |                       |  |
| 2:0                           | BP0_N  | IASK     | the LSBs of the OCM a                                                                                                                                                                        | Selects the number of LSBs of OCM address to mask for the Breakpoint compare, and also the LSBs of the OCM address to keep when using the address substitution. Defines a range of addresses of 2n for "redirecting" the OCM. (n = 0 to 5) |                       |  |
| 4:3                           | BP0_E  | N        | Defines the operation of this Break-Point register set when the OCM addres<br>Break-Point address:<br>00 = Disabled<br>01 = Substitute OCM address (over BP range) with the SUB_ADDR (and OC |                                                                                                                                                                                                                                            | M address matches the |  |
|                               |        |          |                                                                                                                                                                                              |                                                                                                                                                                                                                                            | R (and OCM LSBs)      |  |
|                               |        |          | idress(es)                                                                                                                                                                                   |                                                                                                                                                                                                                                            |                       |  |
|                               |        |          | 11 = Set status and ma                                                                                                                                                                       | 11 = Set status and maskable IRQ on OCM reads from breakpoint address(es)                                                                                                                                                                  |                       |  |
| 15:5                          | Reserv | ved      | Reserved                                                                                                                                                                                     |                                                                                                                                                                                                                                            |                       |  |

| 0xD7C                         | 2            | BP0_OCM            | BP0_OCM_ADDR_hi                                        |  |  |  |  |
|-------------------------------|--------------|--------------------|--------------------------------------------------------|--|--|--|--|
| POD: 0x00                     | 000          |                    |                                                        |  |  |  |  |
| Firmware Breakpoint 0 Address |              |                    |                                                        |  |  |  |  |
| BIT                           | BIT NAME     |                    | FUNCTION                                               |  |  |  |  |
| 7:0                           | BP0_OCM_ADDR | 23:16 bits of 20 b | 23:16 bits of 20 bit breakpoint starting address range |  |  |  |  |
| 15:8                          | Reserved     |                    |                                                        |  |  |  |  |



Interns! BP everything! not drinking



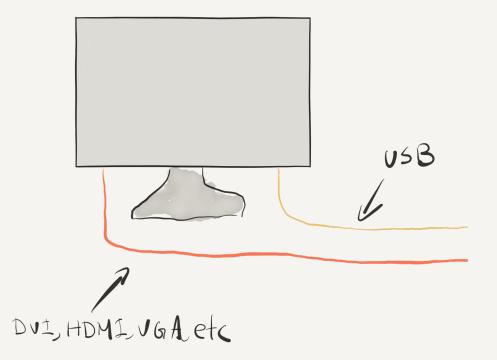
Dumped stack heap load clut, etc API exposed in Pol Congitud)

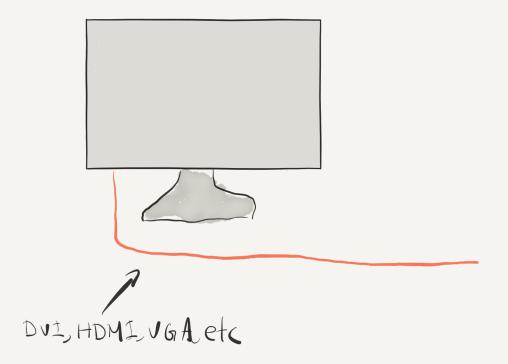
#### 🚺 🚄 🔛

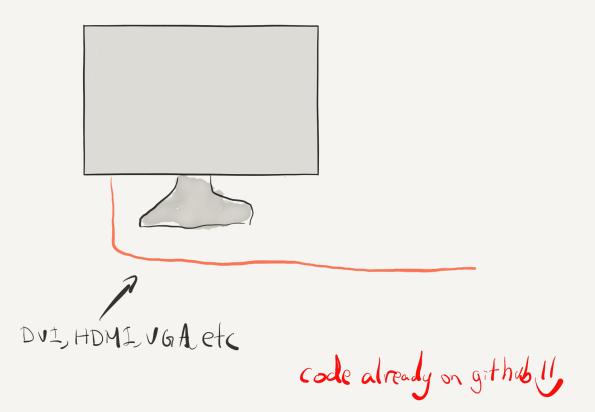
| 00A7FA14                                     |
|----------------------------------------------|
| 00A7FA14                                     |
| <b>OOA7FA14</b> ; Attributes: bp-based frame |
| 00A7FA14                                     |
| 00A7FA14 grab_pixel proc far                 |
| 00A7FA14                                     |
| 00A7FA14 arg_0= word ptr 6                   |
| 00A7FA14 arg_2= word ptr 8                   |
| 00A7FA14 arg_4= word ptr 0Ah                 |
| 00A7FA14                                     |
| 00A7FA14 push bp                             |
| 00A7FA15 mov bp, sp                          |
| 00A7FA17 push si                             |
| 00A7FA18 mov si, [bp+arg_4] ; memory address |
| 00A7FA1B or byte ptr ds:0D6D8h, 1            |
| 00A7FA20 mov ax, [bp+arg_0]                  |
| 00A7FA23 mov ds:0D6DAh, ax                   |
| 00A7FA26 mov ax, [bp+arg_2]                  |
| 00A7FA29 mov ds:0D6DCh, ax                   |
| 00A7FA2C push 2                              |
| 00A7FA2E call far ptr 0A51Ah:0F1h            |
| 00A7FA33 pop cx                              |
| 00A7FA34 mov ax, ds:0D6DEh                   |
| 00A7FA37 mov [si], ax                        |
| 00A7FA39 mov ax, ds:0D6E0h                   |
| 00A7FA3C mov [si+2], ax                      |
| 00A7FA3F mov ax, ds:0D6E2h                   |
| 00A7FA42 mov [si+4], ax                      |
| 00A7FA45 pop si                              |
| 00A7FA46 pop bp                              |
| 00A7FA47 retf                                |
| 00A7FA47 grab_pixel endp<br>00A7FA47         |
| UUR/FR4/                                     |
|                                              |

we find treasure!

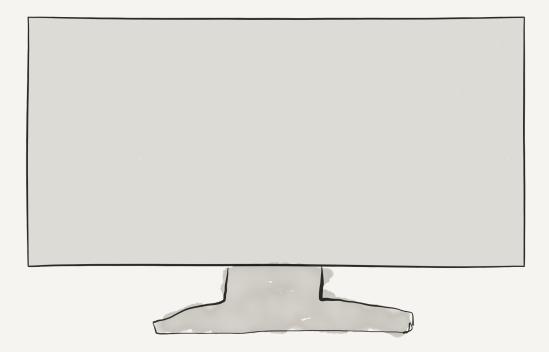




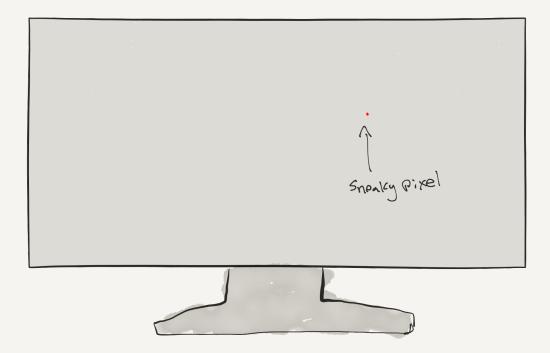




Monitor Implant!

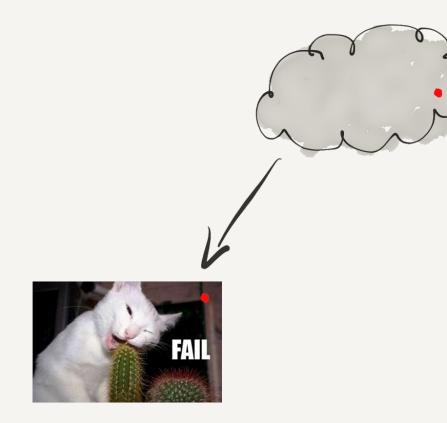


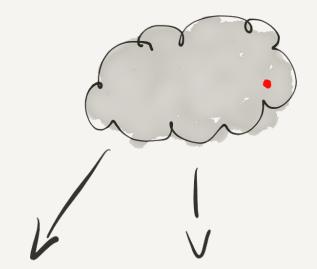
Monitor Implant!



٠

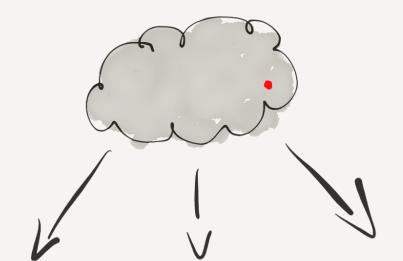










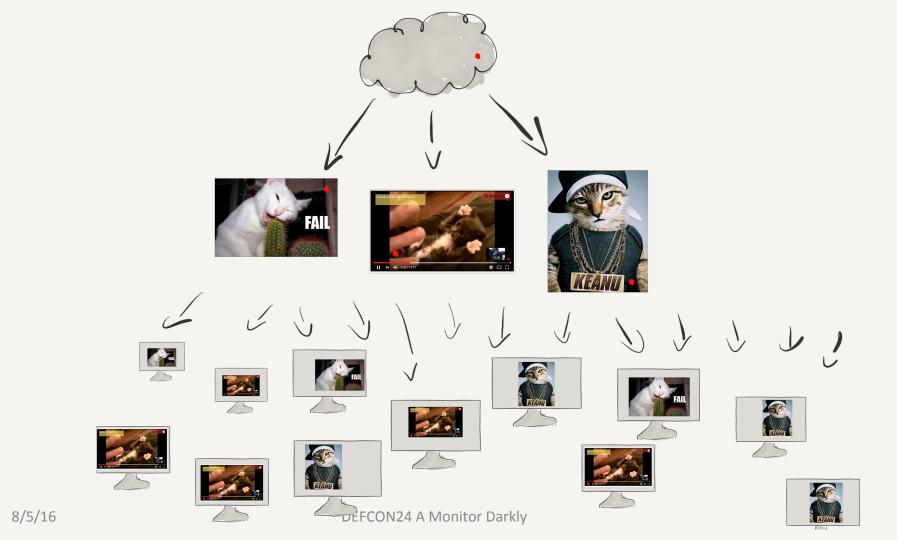




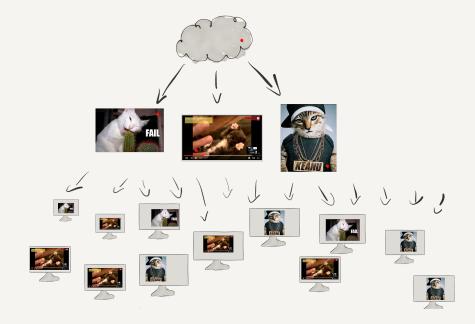




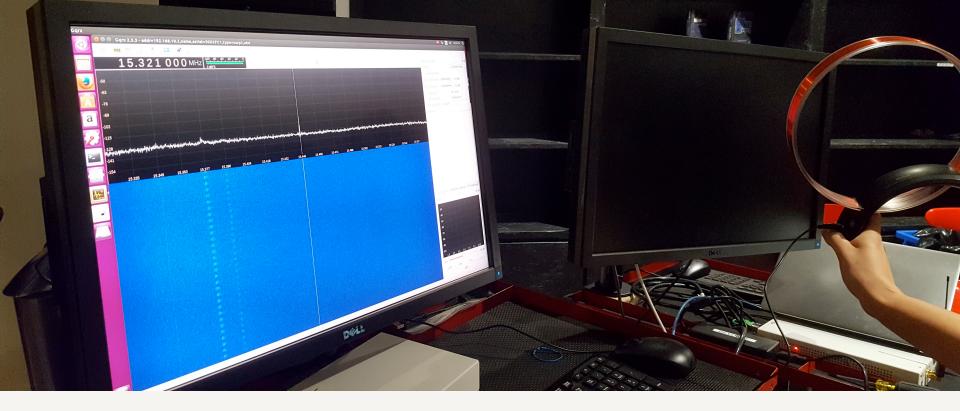
1



Cat-Based World Dominution Plan

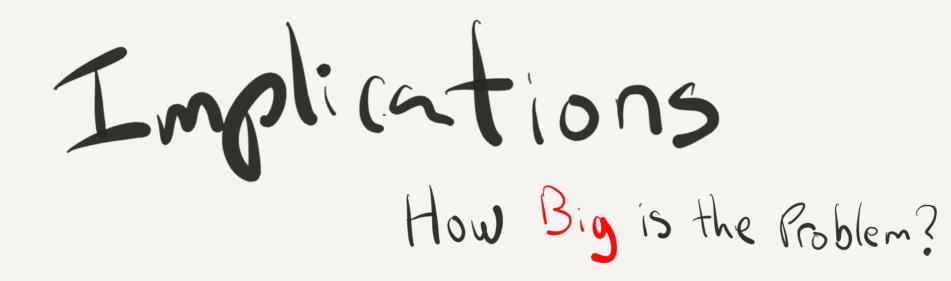


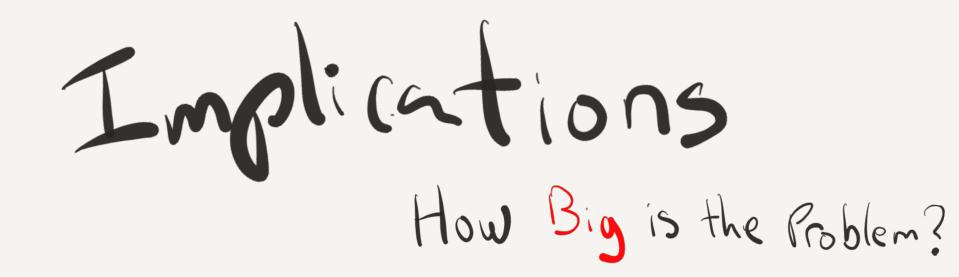
In the end ( Change any Pixel? 2 See every Pixel? 3 Funtena?





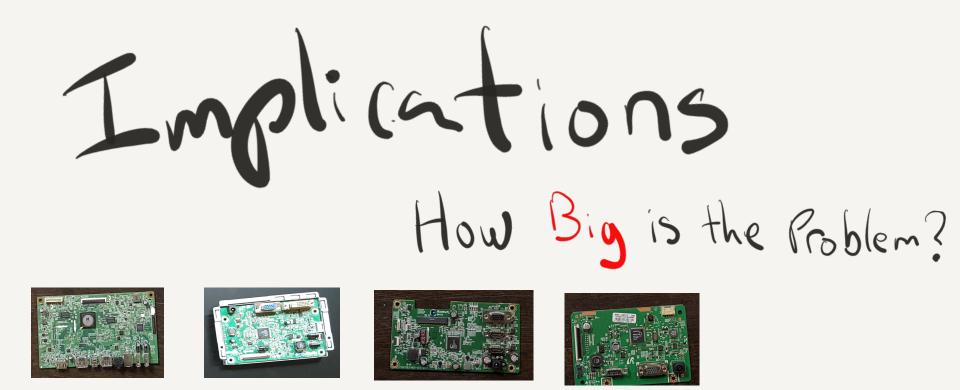




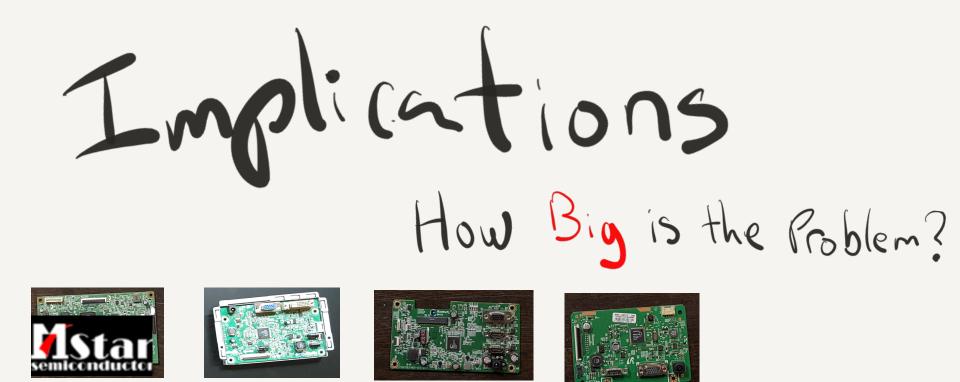




Samsung SE310 Dell 2417U Acer G246HL HP 23xw



8/5/16



8/5/16



Implications How Big is the Problem?

Implications How Big is the Problem?

Implications How Big is the Problem?

#### Flashing a BenQ Z-series for free(dom)

2014-04-28, 00:18 Tech and Hacks

DISCLAIMER: If you attempt to reflash your screen's firmwathat you end up with a very expensive brick. As always, I ca

## Alexandre Boeglin

```
http://boeglin.org/blog/index.php?
entry=Flashing-a-BenQ-Z-series-for-
free(dom)
```

# HTTPS://GITHUB.COM/REDBALLOONSHENANIGANS/MONITORDARKLY

please Contribute.

Let's try to fix the problem



Work with Cool Kids Build Embedded Security Tech Protect All The Things Jobs Credballoonse writy. Com

ThanKS Big



Amazing Interns!

Boß Lumsden

Connor Abbo

Brian Hong



DELL DOES NOT YET HAVE A SECURITY FIX AGAINST SHAK ATTACK



MANY MONITORS Were Harmed In the Making Of This Presentation

CHRIS LIVES HAPPILY WITH HIS SEMI-UNMODIFIED 34" MONITOR